Drax 11.6" Schematic

SKL-Y

2016-03-21

REV : A00

DY : None Installed

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Title	***Cover Page***	
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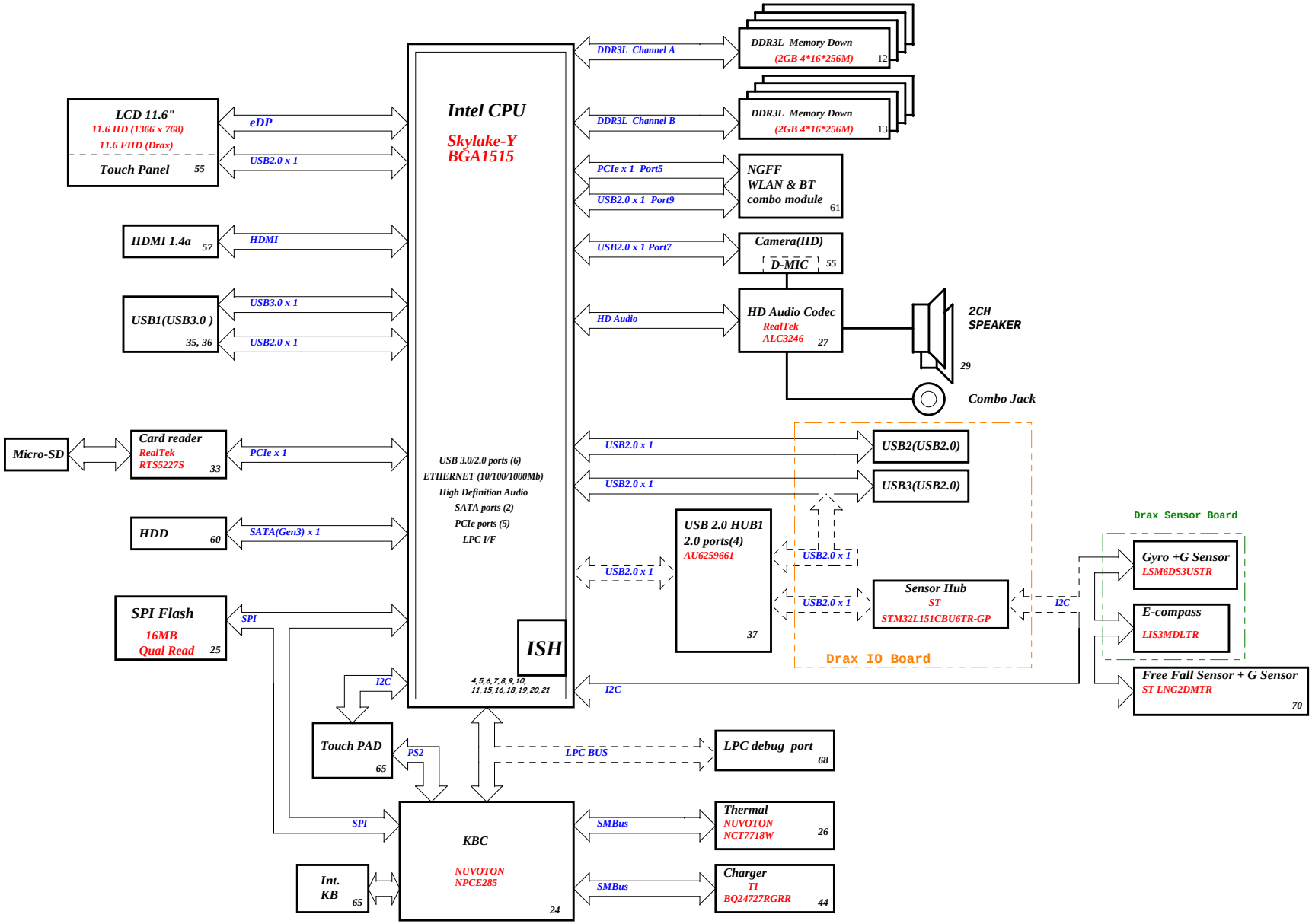
Project code : 4PD06Q010001
PCB P/N : 15250
Revision : A00

Drax 11.6" Block Diagram



CHARGER BQ24727RGRR 44	
INPUTS	OUTPUTS
19V_DCBATOUT	12V_BT+

SYSTEM DC/DC SY8288CRAC SY8286BRAC 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power NCP81208MNTXG NCP81381MNTXG *2 SY8288RAC NCP81253MNTBG 46-50	
INPUTS	OUTPUTS
19V_DCBATOUT	+VCC_CORE +VCCGT 1D0V_S5 +VCCSA

DDR3L SUS SY8288RAC APL5338XAI 51	
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_S3 0D675V_S0

SYSTEM DC/DC APL5930KAI 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

PCB LAYER

L1:Top	L5:Signal
L2:Signal	L6:GND
L3:GND	L7:Signal
L4:Signal	L8:Bottom

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Title: Block Diagram

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SSID = CPU

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

+VCCSTG
+VCCST_CPU
R427 1KR2J-1-GP H_PROCHOT#
R429 1KR2J-1-GP
THERMTRIP# CPU_R
EC401 DY AZ5725-01FDR7G-GP

[24] H_PECI
[24,44,46] H_PROCHOT#
499R2F-2-GP R415
60D4R2F-GP R421
TP417 TP416
CATERR# CPU
PROCHOT# CPU
THERMTRIP# CPU
SKTOCC# CPU

[99] BPM_CPU_N0
[99] BPM_CPU_N1
TP415 TP414
BPM_CPU_N0
BPM_CPU_N1
BPM_CPU_N2
BPM_CPU_N3

TOUCHPAD_INTR#

49D9R2F-GP R422
49D9R2F-GP R428
CPU_POPIRCOMP
PCH_POPIRCOMP

CPU1D 4 OF 20
SKYLAKE_ULX
H49 CATERR#
F49 PECI
J48 PROCHOT#
H47 THERMTRIP#
B62 SKTOCC#
H51 BPM#[0]
J50 BPM#[1]
F51 BPM#[2]
G50 BPM#[3]
E11 GPP_E3/CPU_GP0
M9 GPP_E7/CPU_GP1
BD8 GPP_B3/CPU_GP2
BC11 GPP_B4/CPU_GP3
BN17 PROC_POPIRCOMP
BP16 PCH_OPIRCOMP
CPU MISC
JTAG
D53 PROC_TCK — XDP_TCK_CPU [99]
C54 PROC_TDI — XDP_TDI_CPU [99]
G48 PROC_TDO — XDP_TDO_CPU [99]
C59 PROC_TMS — XDP_TMS_CPU [99]
F47 PROC_TRST# — XDP_TRST#_CPU [99]
B53 PCH_JTAG_TCK — PCH_JTAG_TCK [99]
C50 PCH_JTAG_TDI — PCH_JTAG_TDI [99]
B51 PCH_JTAG_TDO — PCH_JTAG_TDO [99]
A52 PCH_JTAG_TMS — PCH_JTAG_TMS [99]
C52 PCH_TRST# — XDP_TRST#_CPU [99]
B49 JTAGX — XDP_TCK_JTAGX [99]
SKYLAKE-Y-GP

071.SKYLA.0C0U
PV stage CPU

3D3V_S5_PCH
R404 DY 100KR2J-1-GP
3D3V_S0
R406 DS3 100KR2J-1-GP

NON DS3
R410 0R0402-PAD-1-GP
A00 20160302
DS3 D401 RB751V-40H-GP
K A
[24,65] INT_TP#
83.R2004.G8F

Add resistor by NON DS3 function

+VCCSTG
PCH_JTAG_TMS R438 51R2J-2-GP
PCH_JTAG_TDI R439 51R2J-2-GP
XDP_TCK_JTAGX R430 DY 1KR2J-1-GP
PCH_JTAG_TDO R440 51R2J-2-GP
PCH_JTAG_TCK R437 DY 51R2J-2-GP

+VCCSTG
XDP_TMS_CPU R433 DY 51R2J-2-GP
XDP_TDI_CPU R434 DY 51R2J-2-GP
XDP_TDO_CPU R435 DY 51R2J-2-GP
XDP_TCK_CPU R431 51R2J-2-GP
XDP_TRST# CPU R436 DY 51R2J-2-GP

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Title: CPU (JTAG/CPU SIDE BAND)
Size: A4 | Document Number: Drax SKL Y | Rev: A00
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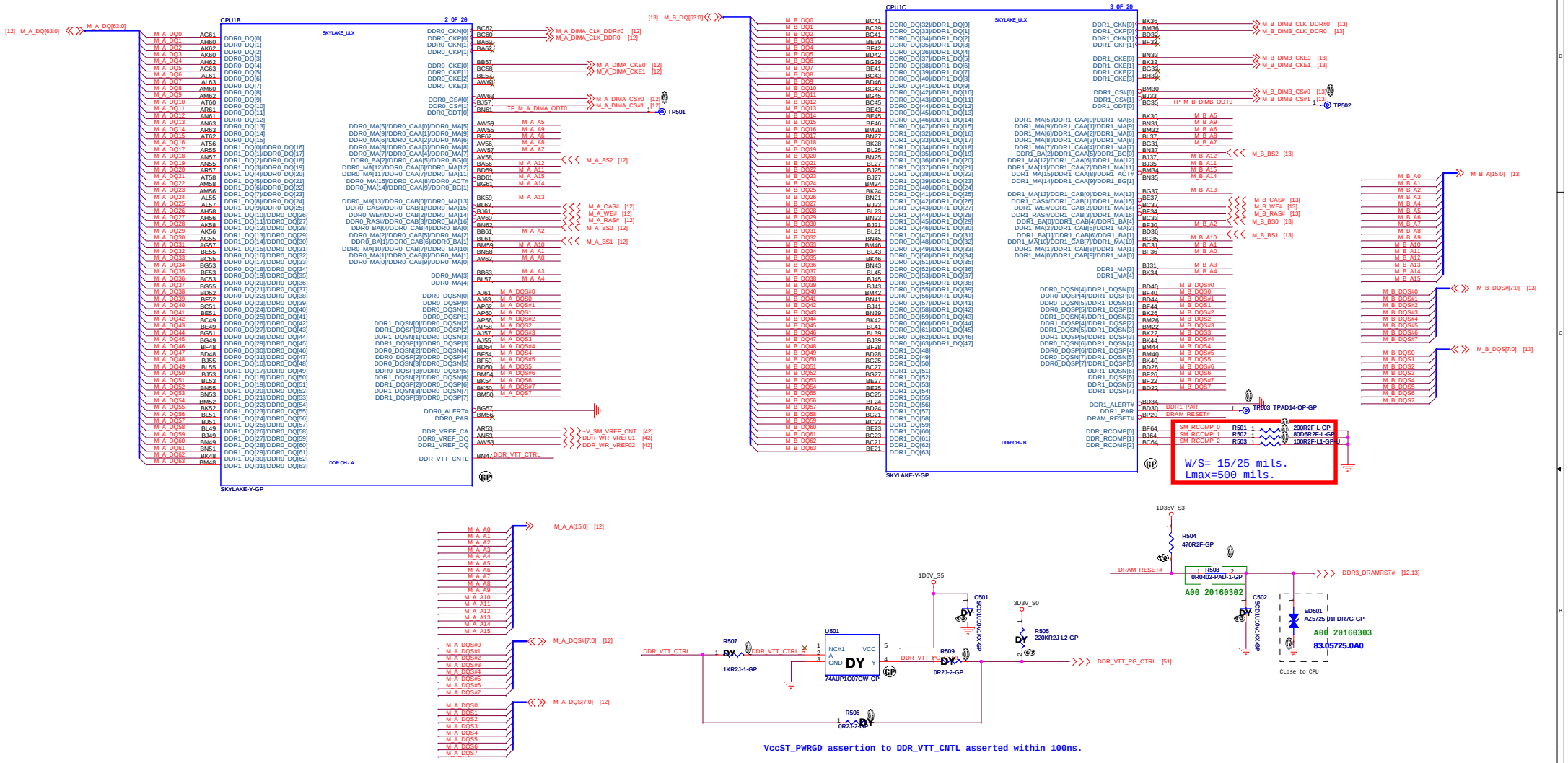
SSID = CPU



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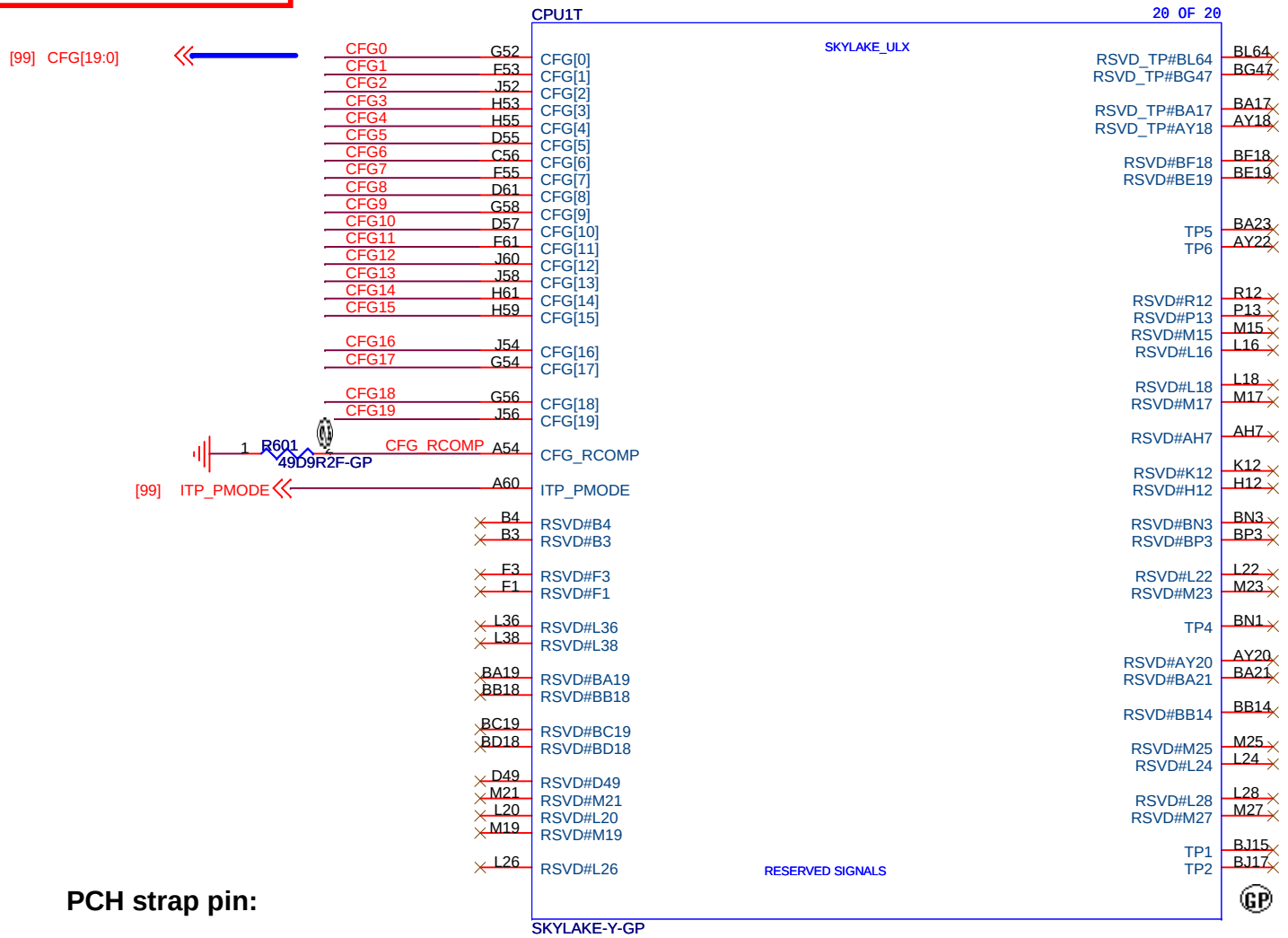
Title: CPU(DDR)

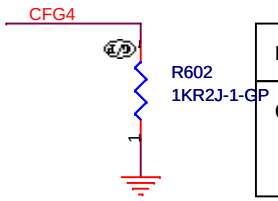
Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Monday, March 21, 2016 | Sheet 5 of 109

SSID = CPU



PCH strap pin:



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title: CPU (CFG/RSVD)

Size: A4 | Document Number: Drax SKL Y | Rev: A00

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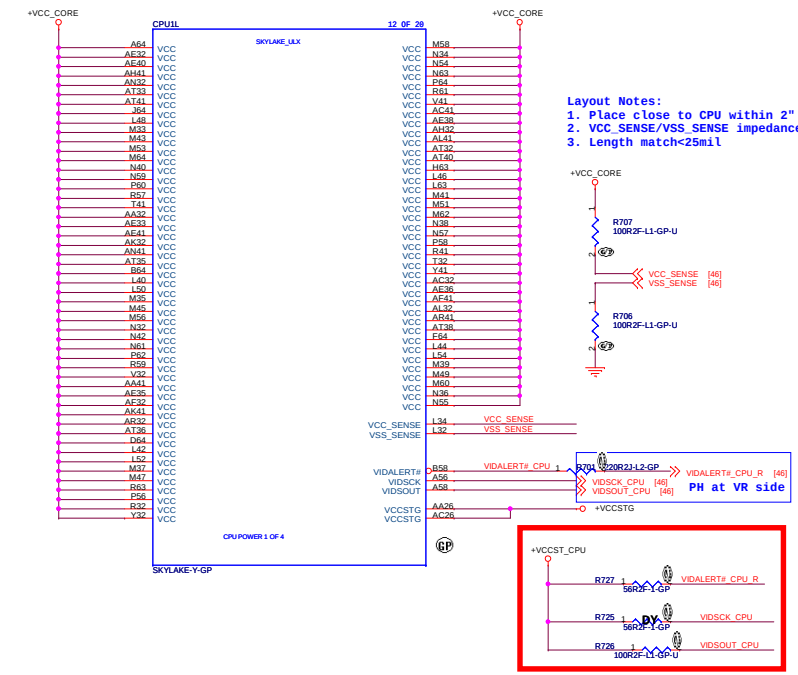
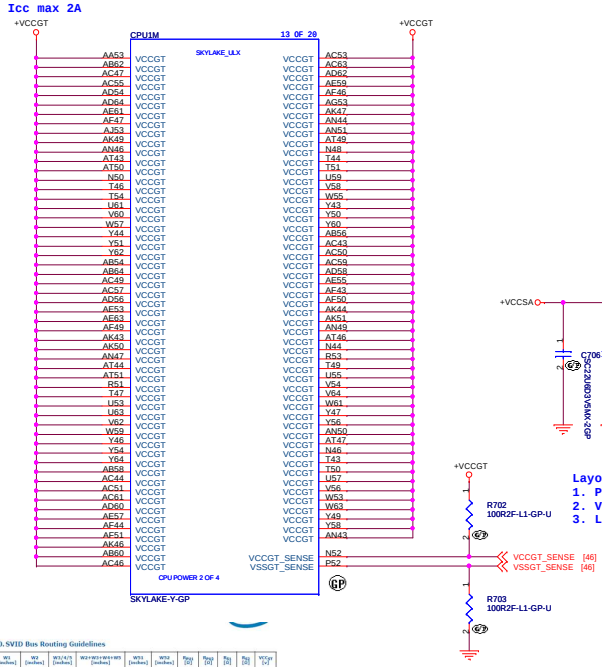
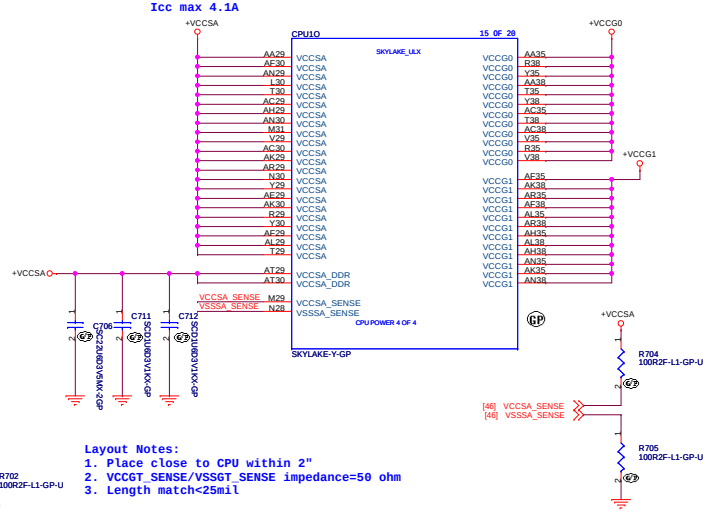
SSID = CPU



Layout Notes:
1. Place close to CPU within 2"
2. VCC_SENSE/VSS_SENSE impedance=50 ohm
3. Length match<25mil



Layout Notes:
1. Place close to CPU within 2"
2. VCCGT_SENSE/VSSGT_SENSE impedance=50 ohm
3. Length match<25mil



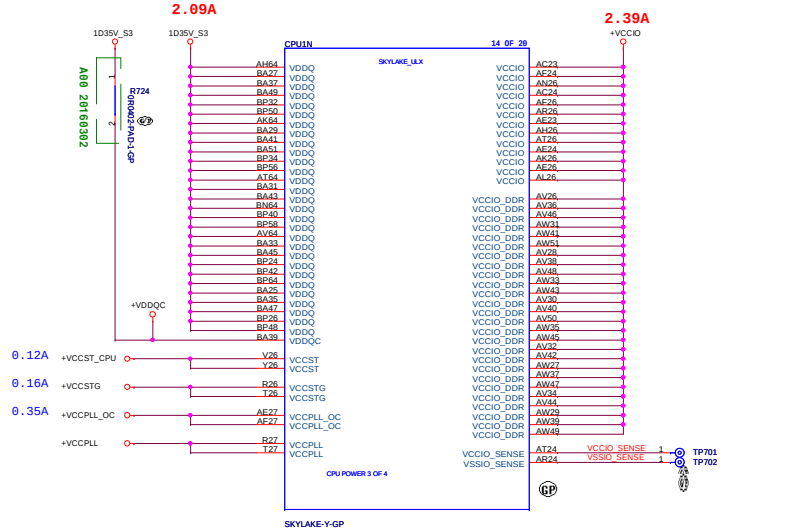
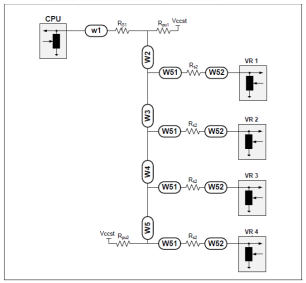


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 (inches)	W2 (inches)	W3/4/5 (inches)	W2+W3+W4+W5 (inches)	W51 (inches)	W52 (inches)	Rpu (Ω)	Rpd (Ω)	Rsh (Ω)	Rsh (Ω)	VCCst (V)
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management please refer to *Chapter 51, "Power Architecture Guide"* in this document.



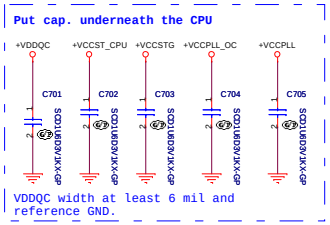
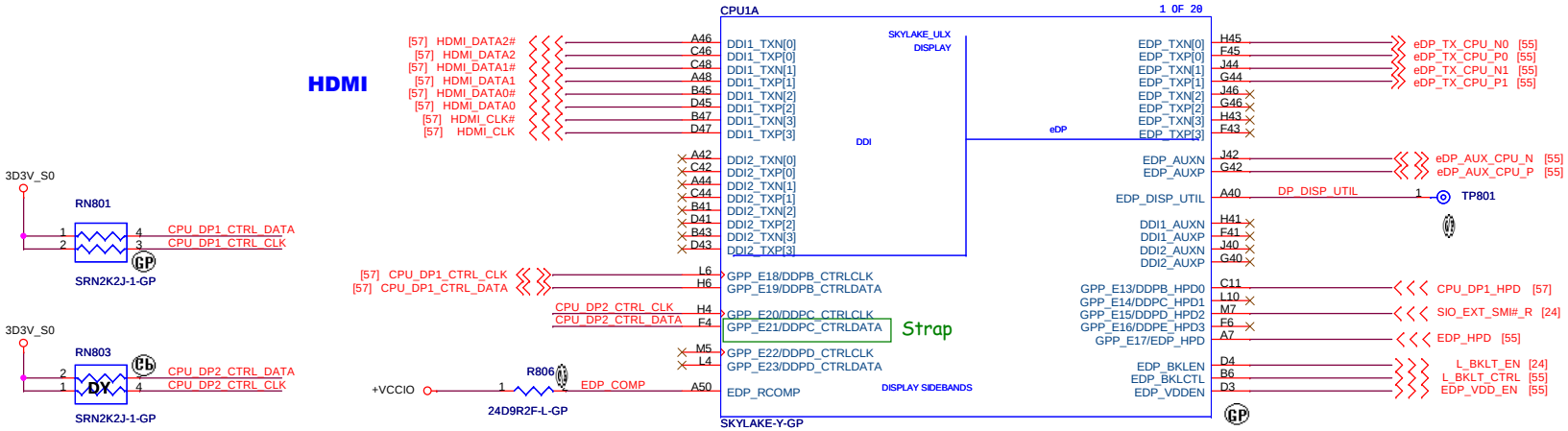


Table 52-2. Decoupling Requirements for Skylake Y Processor (Sheet 2 of 4)

Domain	Backside Cap	Primary Side Cap	Placement Guideline
V_{DDQC}	1x 0.1 uF 0201		Filter implemented between VDDQC and VDDQ. Capacitor tapped directly to VDDQC first and connect to VDDQ through L (routed as trace). Please refer to Figure 66-6 for details.
Vcc_{SA_DDR}	1x 0.1 uF 0201		Place on secondary side, underneath the package Refer to Note 4 for component placement
		1x 22 uF 0603	Place as close to the package as possible
Vcc_{PLL_OC}	1x 0.1 uF 0201		Place on secondary side, underneath the package Please refer to Figure 52-4 below. Do not route Vcc_{PLL_OC} closest adjacent layer over any power net other than ground.
Vcc_{PLL}	1x 0.1 uF 0201		Place on secondary side, underneath the package Please refer to Figure 52-5 below. Do not route Vcc_{PLL}, Vcc_{ST}, Vcc_{STG} closest adjacent layer over any power net other than ground.
Vcc_{ST} [7]	1x 0.1 uF 0201		
Vcc_{STG} [8]	1x 0.1 uF 0201		

SSID = CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

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Title: CPU (DISPLAY)

Size: A3 | Document Number: Drax SKL Y | Rev: A00

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SSID = CPU

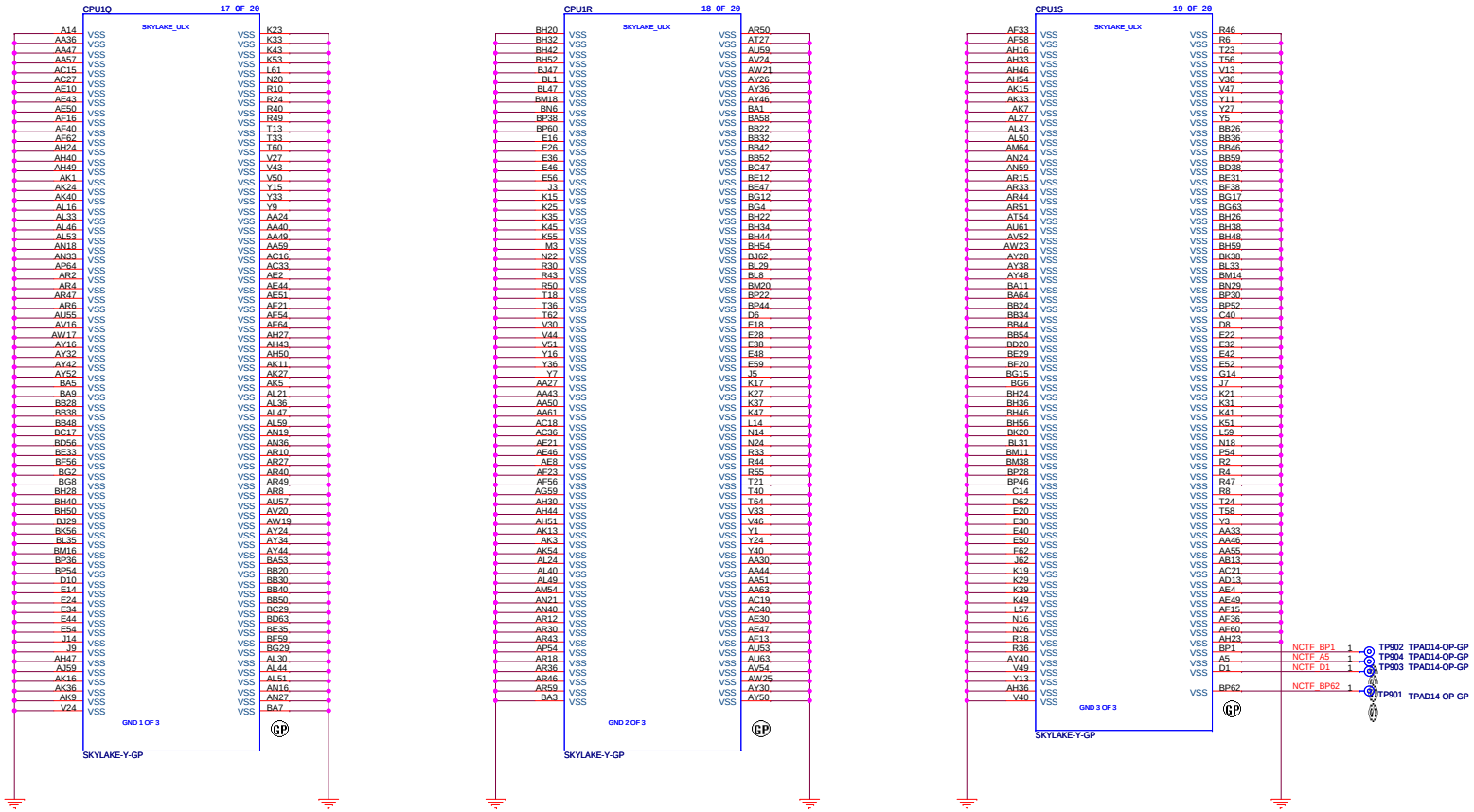

Table 45-3. Skylake Y Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BP64	NCTFVDDQ	Test Point (TP)	Corner BP64
BN64	NCTFVDDQ	Test Point (TP)	
BP62	NCTFVSS	Test Point (TP)	
BP1	NCTFVSS	Test Point (TP)	Corner BP1
D1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A64	NCTFVCC	Test Point (TP)	Corner A64
B64	NCTFVCC	Test Point (TP)	

Note: Refer to Processor EDS for more details on NCTF information.

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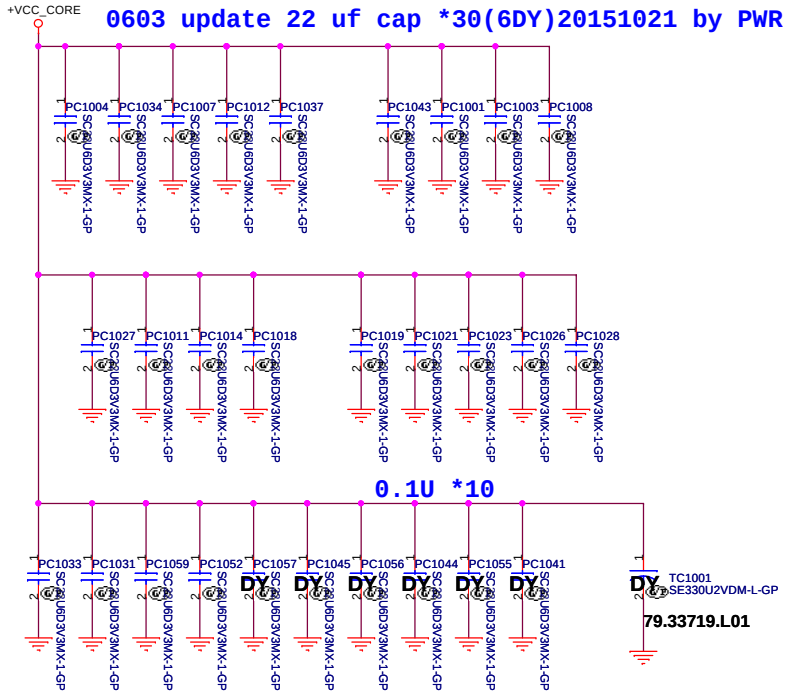
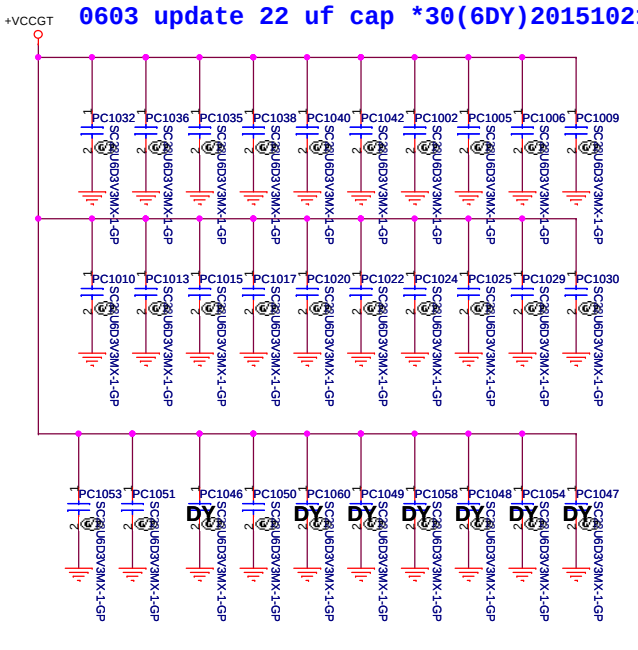
Title: CPU (VSS)

Size: C | Document Number: Drax SKL Y | Rev: A00

Date: Monday, March 21, 2016 | Sheet 9 of 109

SSID = CPU





Decoupling Requirements for SKL Y Processor (Sheet 1 of 4)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{GT}	12x 0.1uF 0201		Place on secondary side, underneath the package Refer to Note 2 for component placement
	40x 0.1uF 0201 (Placeholder)		
		2x 1uF 0402	Place as close to the package as possible. Placement order: Package edge > 0402 1uF caps > 0402 10uF caps >0805 caps > Power source
		2x 10uF 0402 (Placeholder)	
		9x 47uF 0805 (6.3V)[1]	
Vcc	20x 0.1uF 0201		Place on secondary side, underneath the package Refer to Note 3 for component placement
	12x 0.1uF 0201 (Placeholder)		
		8x 10uF 0402	Place as close to the package as possible. Placement order: Package edge > 0402 caps > 0805 caps > Power source
		6x 47uF 0805 (6.3V)[1]	
		2x 47uF 0805 (Placeholder)	

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Title: CPU (Power CAP1)

Size: A3 | Document Number: Drax SKL Y | Rev: A00

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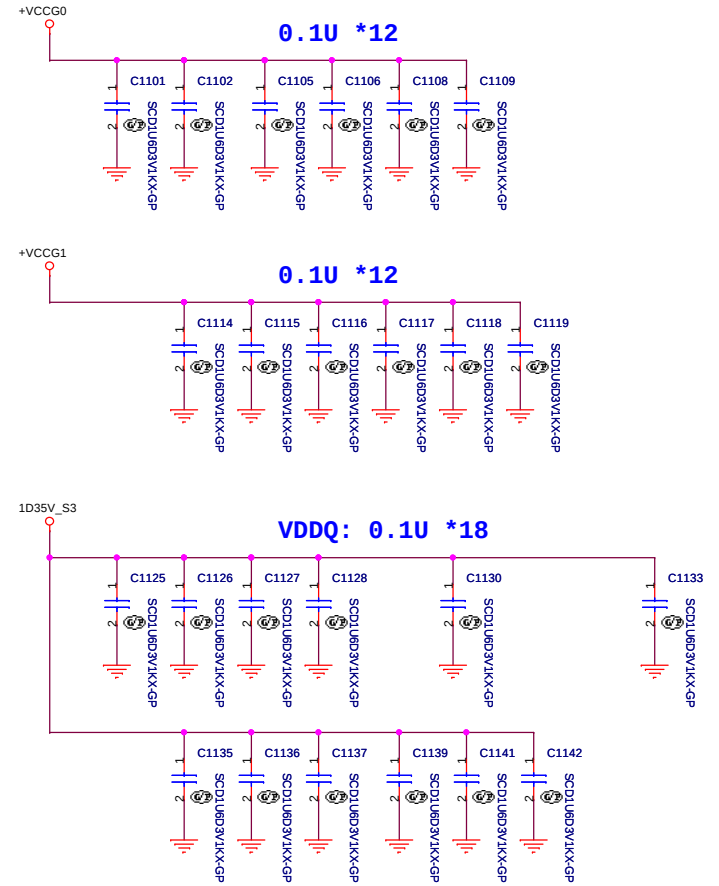
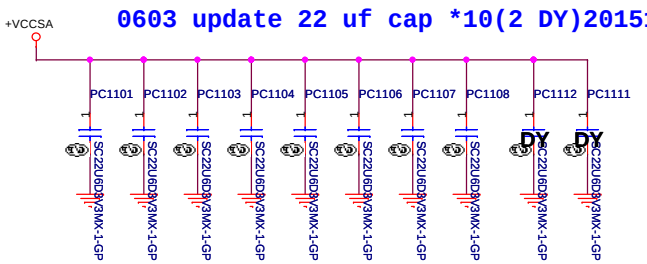
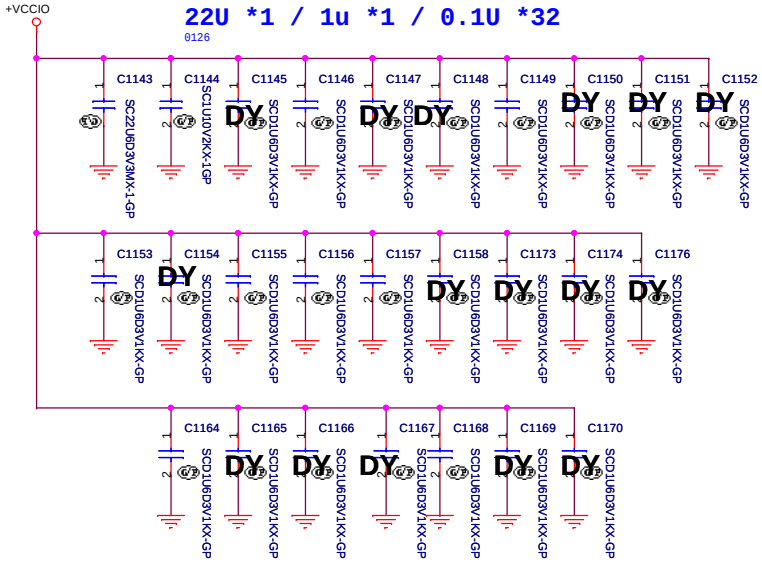
SSID = CPU







Decoupling Requirements for Skylake Y Processor (Sheet 2 of 4)

Domain	Backside Cap	Primary Side Cap	Placement Guideline
Vcc_{G0}	12x 0.1 uF 0201		Place on secondary side, underneath the package
Vcc_{G1}	12x 0.1 uF 0201		Place on secondary side, underneath the package
V_{DDQ}	18x 0.1 uF 0201		Place on secondary side, underneath the package
V_{DDQC}	1x 0.1 uF 0201		Filter implemented between VDDQC and VDDQ. Capacitor tapped directly to VDDQC first and connect to VDDQ through L (routed as trace). Please refer to Figure 66-6 for details.
Vcc_{IO}	13x 0.1 uF 0201		Isolation between DDR and display area. Place on secondary side, underneath the package Please refer to Figure 52-1 below
		1x 1 uF 0402	Place as close to the package as possible. Placement order: Package edge > 0402 caps > 0805 caps > Power source
Vcc_{SA}	1x 1 uF 0201		Place on secondary side, underneath the package Refer to Note 4 for component placement Please refer to Figure 52-3 below
		4x 22 uF 0603	Place as close to the package as possible

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Title: CPU (Power CAP2)

Size: A3 | Document Number: Drax SKL Y | Rev: A00

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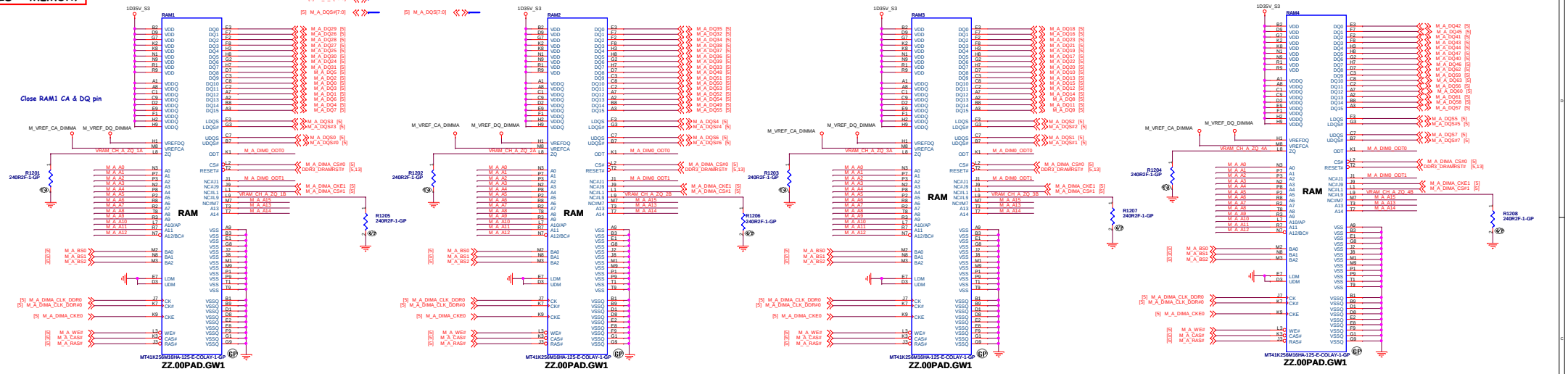
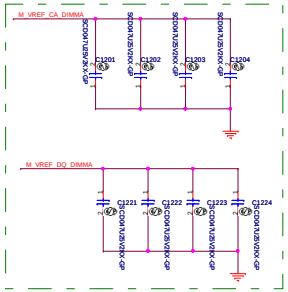
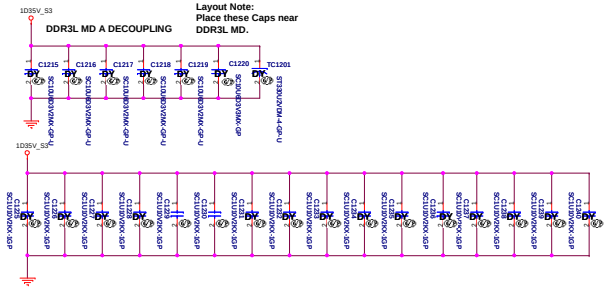
SSID = MEMORY

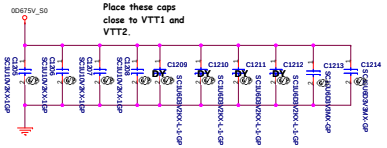




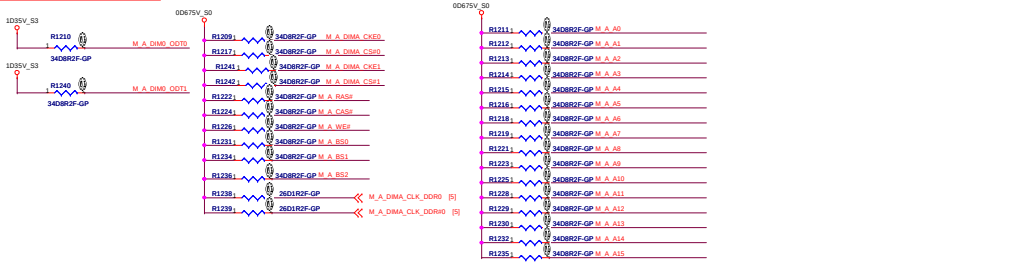
DIMM VREF FILTER CAPS

PLACE THESE CAPS NEAR TO RESPECTIVE DIMM PINS

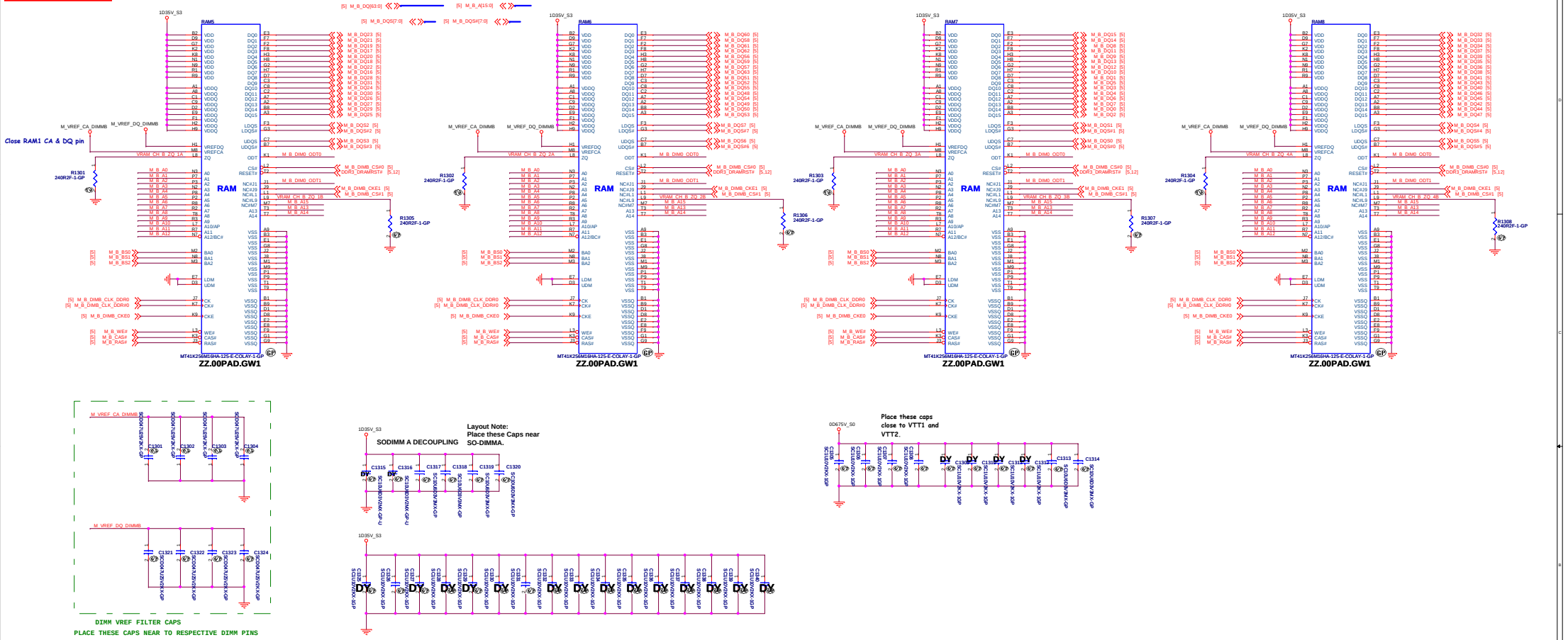




SSID = MEMORY

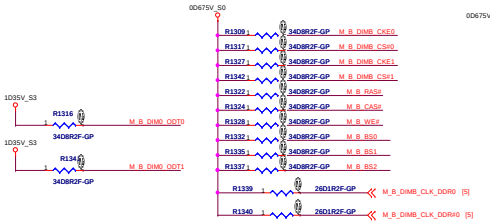


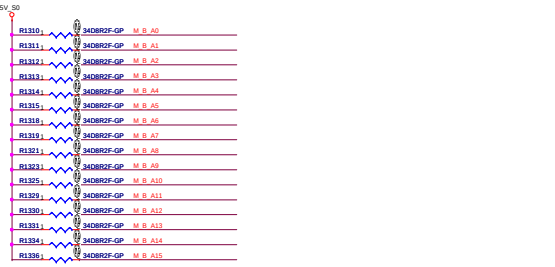
SSID = MEMORY



DIMM VREF FILTER CAPS

PLACE THESE CAPS NEAR TO RESPECTIVE DIMM PINS





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Title: DDR3L-Memorydown2

Size: Custom | Document Number: Drax SKL Y | Rev: A00

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Title	***Reserved***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
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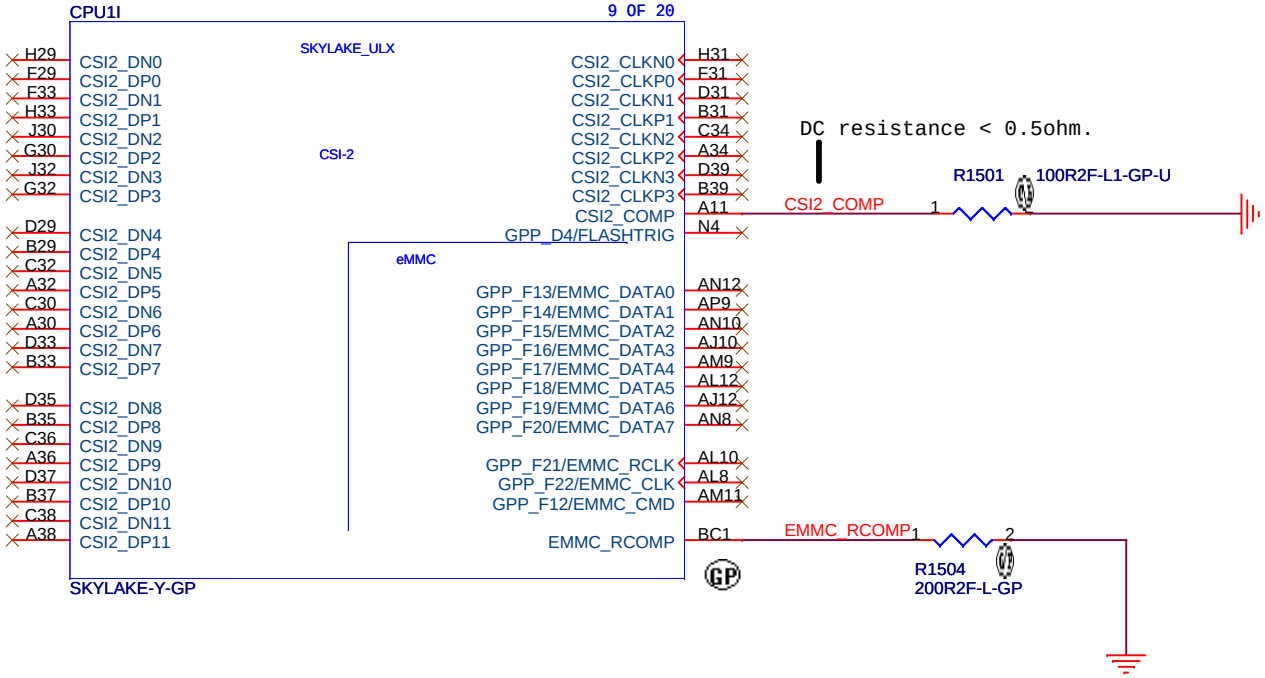
SSID = CPU



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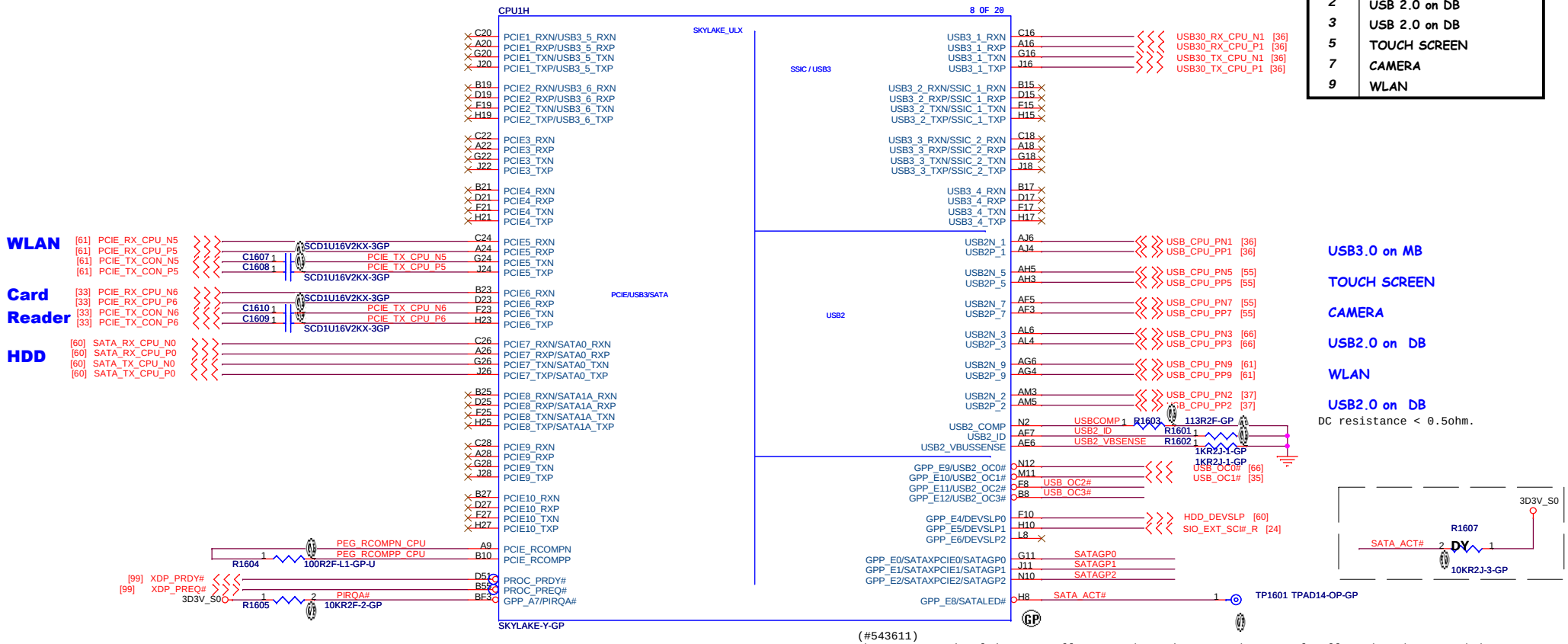
Title	CPU (CSI2/EMMC)	
Size A4	Document Number Drax SKL Y	Rev A00
Date: Monday, March 21, 2016	Sheet 15 of 109	

SSID = PCH

USB Table

Pair	Device
1	USB3.0 on MB
2	USB 2.0 on DB
3	USB 2.0 on DB
5	TOUCH SCREEN
7	CAMERA
9	WLAN



(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

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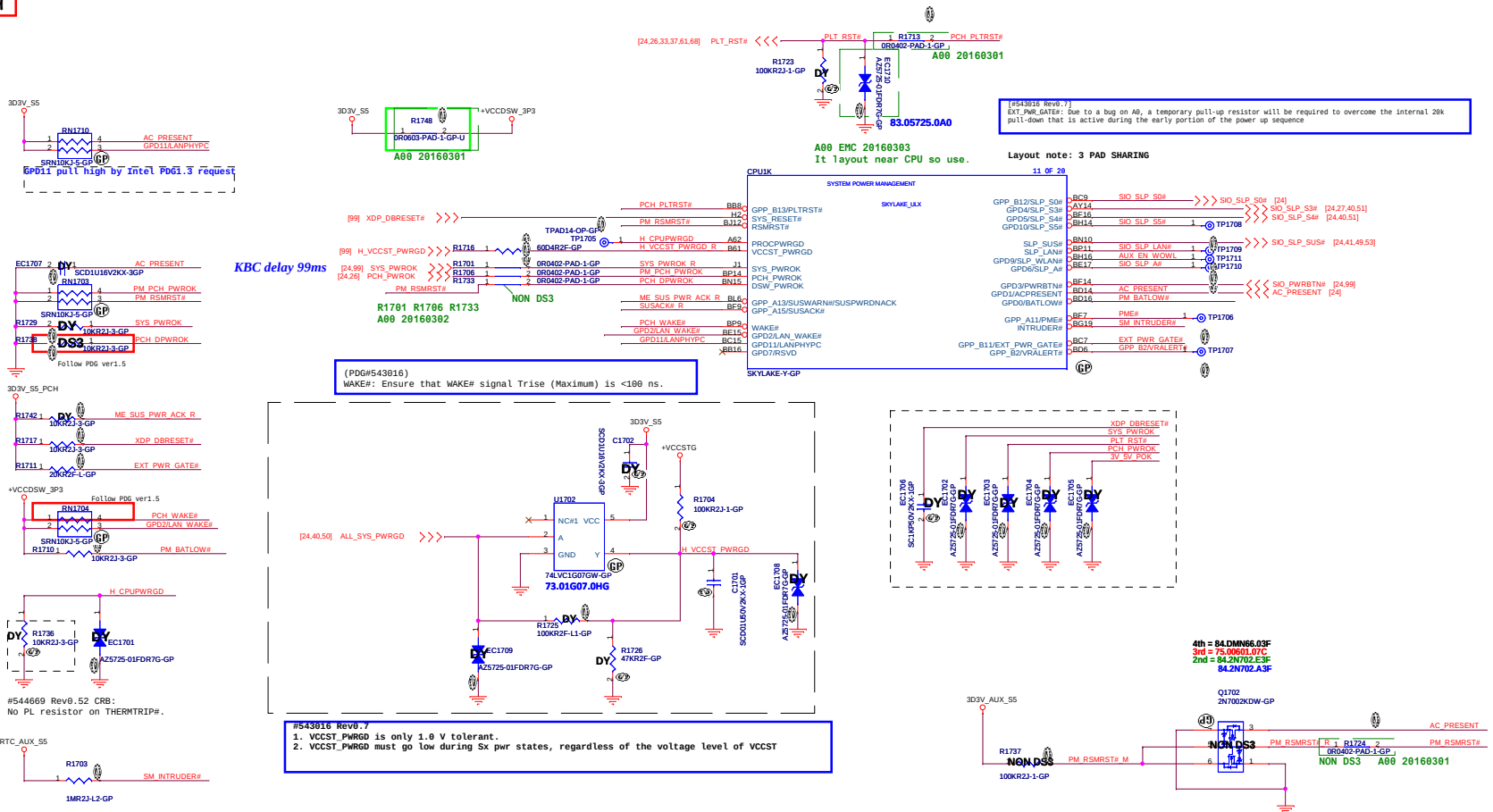
Title: CPU (PCIE/SATA/USB)

Size: A3 | Document Number: Drax SKL Y | Rev: A00

Date: Thursday, March 17, 2016 | Sheet 16 of 109

SSID = PCH



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Title: CPU (PM)

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Monday, March 21, 2016 | Sheet 17 of 109

SSID = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

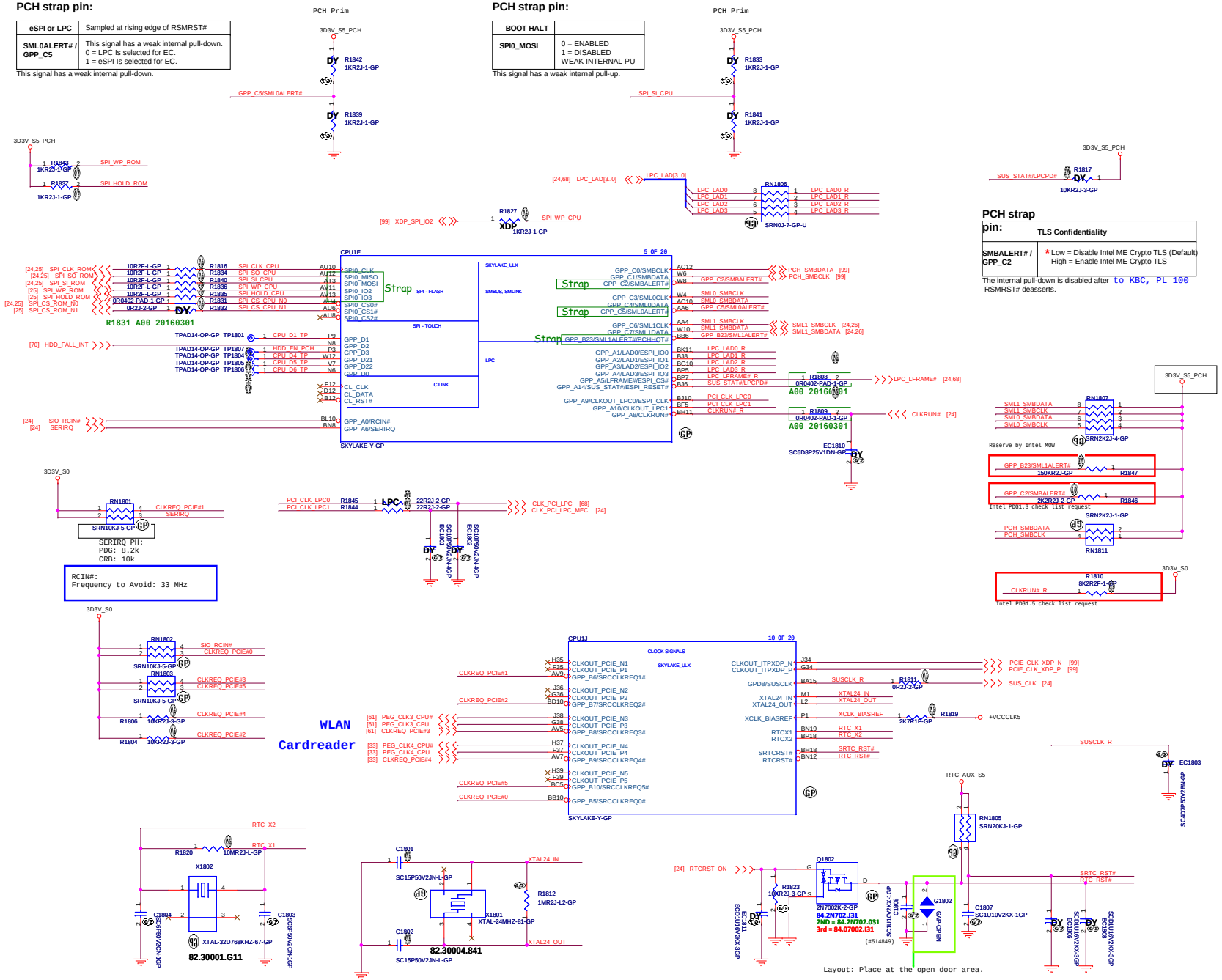
BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH strap pin:

TLS Confidentiality	
SMBALERT# / GPP_C2	* Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts. to KBC, PL 100



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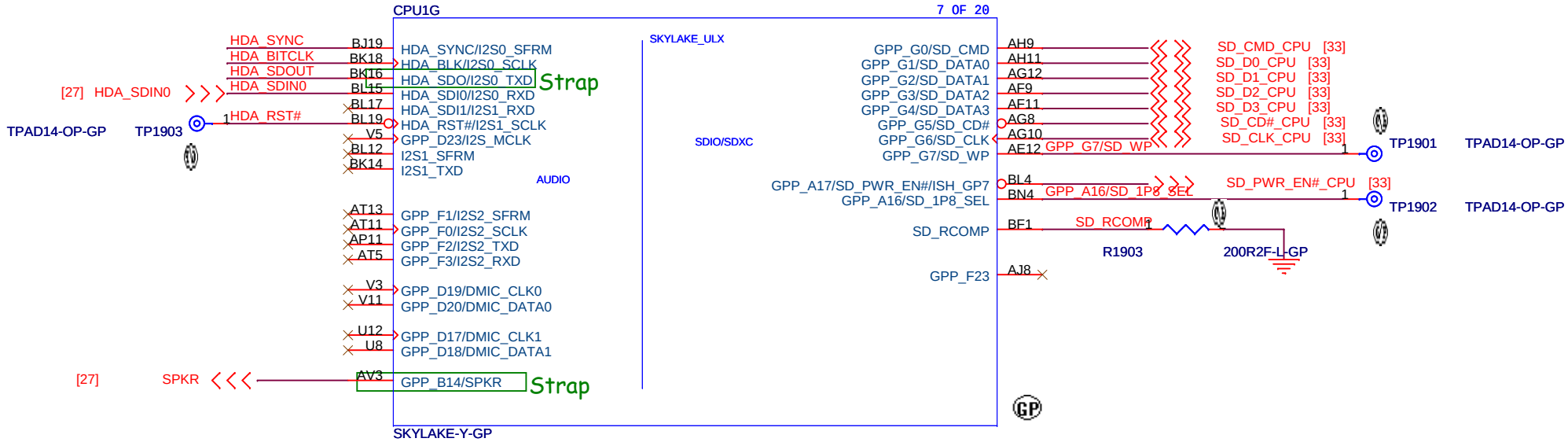
Title: CPU (LPC/SPI/SMBS/RTC/CLK)

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Monday, March 21, 2016 | Sheet 18 of 109

SSID = PCH



PCH strap pin:

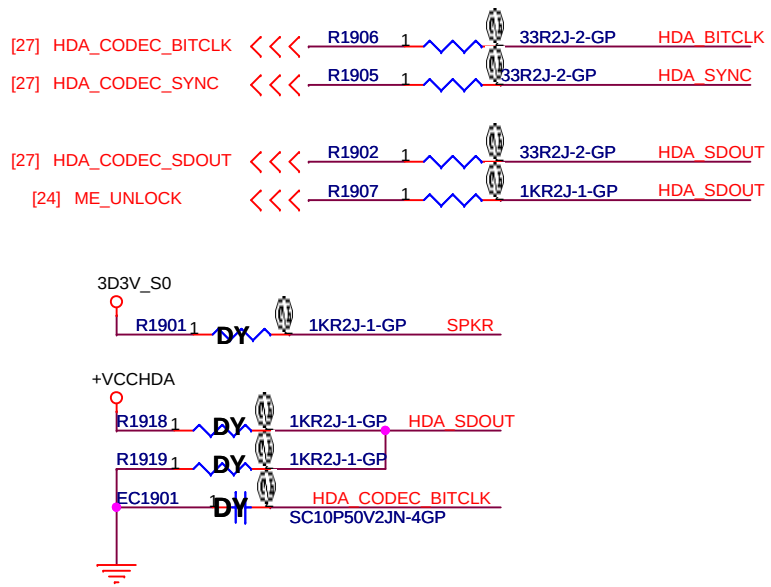
NO REBOOT	
HDA_SPKR	Low = Enable (Default) * High = Disable

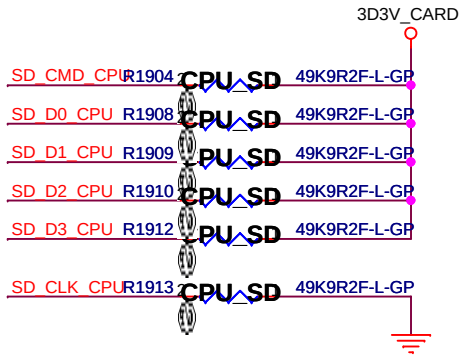
The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts





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Title		
CPU (AUDIO/SDIO)		
Size A4	Document Number Drax SKL Y	Rev A00
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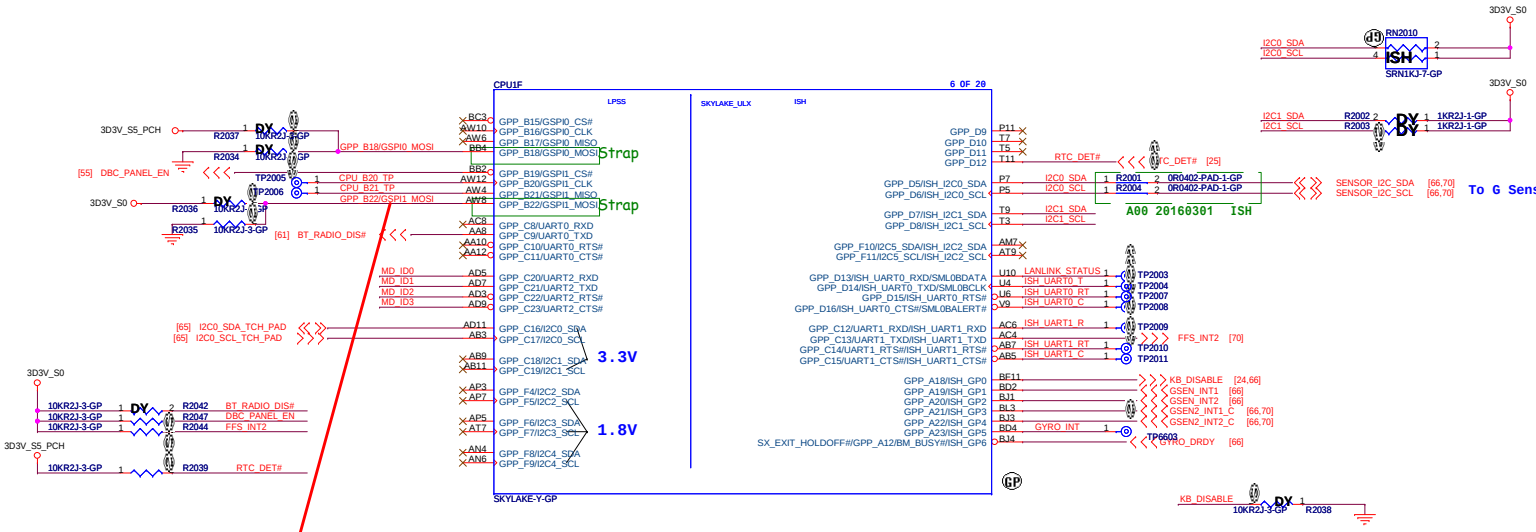
SSID = PCH



PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

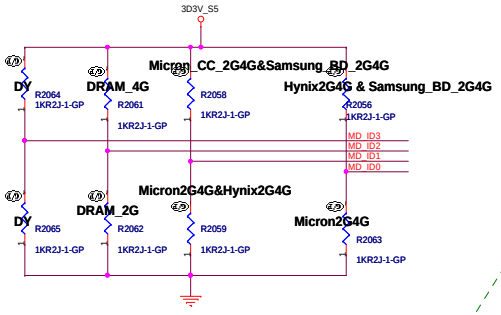
Need double confirm, GPIO table set to GPI if that's needed PH or PL

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	* 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

Memory Down Strap



A00 20160302

RAM ID bit order is DRAM_ID2,DRAM_ID1,DRAM_ID0

Vender	RAM_ID	Wistron PN	Mfr. PN	Capacity	Freq
Micron	X000	NX80R$CB	MT41K256M16LY-107:N	2G	1600MHz
Hynix	X001	NX80R$AB	H5TC4G63CFR-PBA	2G	1600MHz
Micron	X010	NX80R$CC	MT41K256M16T	2G	1600MHz
Samsung	X011	NX80R$BD	K4B4G1646E-BYK0	2G	1600MHz
Micron	X100	NX80R$CB	MT41K256M16LY-107:N	4G	1600MHz
Hynix	X101	NX80R$AB	H5TC4G63CFR-PBA	4G	1600MHz
Micron	X110	NX80R$CC	MT41K256M16T	4G	1600MHz
Samsung	X111	NX80R$BD	K4B4G1646E-BYK0	4G	1600MHz

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Title: CPU (LPSS/ISH/I2C/UART/GPIO)

Size: C | Document Number: Drax SKL Y | Rev: A00

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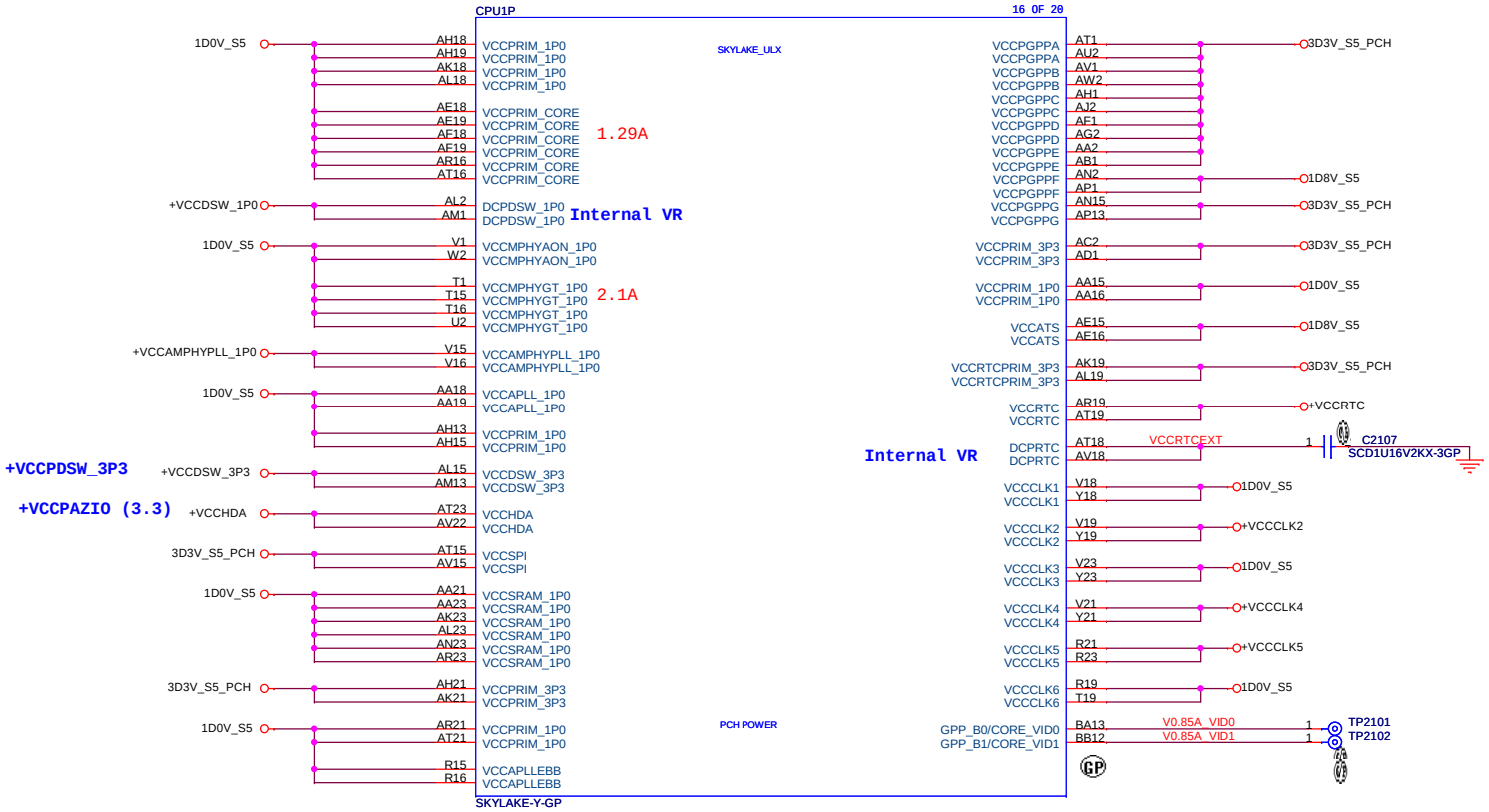
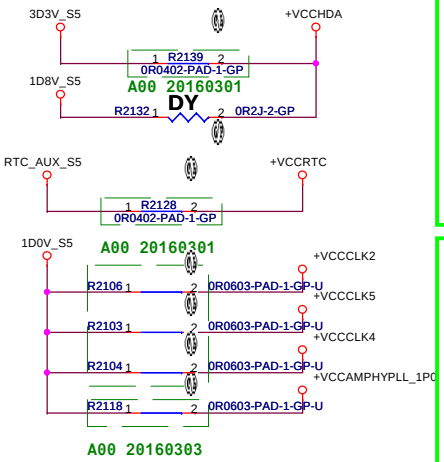
SSID = PCH



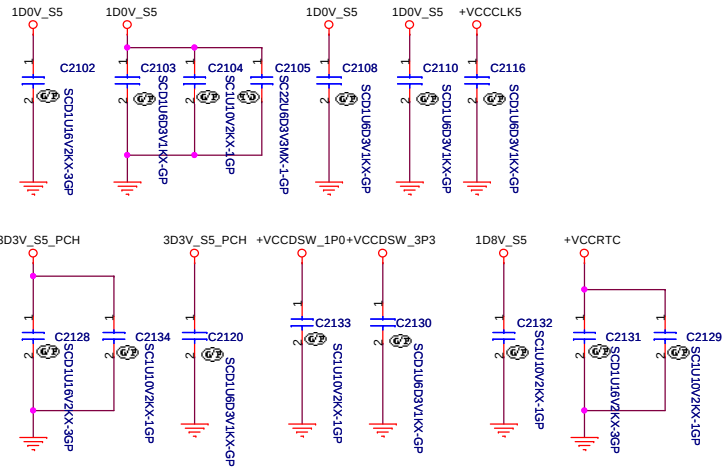


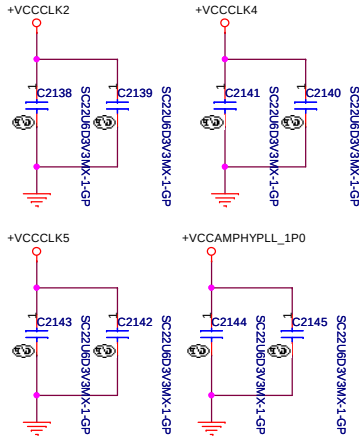
Layout Note:

D1uF:
C2102 near V1
C2103 near T1, T15
C2108 near AH13, AH15
C2110 near R15, R16
C2116 near R21
1uF:
C2104 near T1, T15
22uF:
C2105 near T1, T15

Layout Note:

D1uF:
C2128 near AK19
C2120 near AT15
C2130 near AL15
C2131 near AR19
1uF:
C2134 near AK19
C2129 near AR19
C2132 near AE15
C2133 near AL2





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Title	PCH (POWER1)	
Size A3	Document Number Drax SKL Y	Rev A00
Date: Thursday, March 17, 2016	Sheet 21 of 109	

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Title

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Size	Document Number	Rev
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Date: Thursday, March 17, 2016 Sheet 22 of 109

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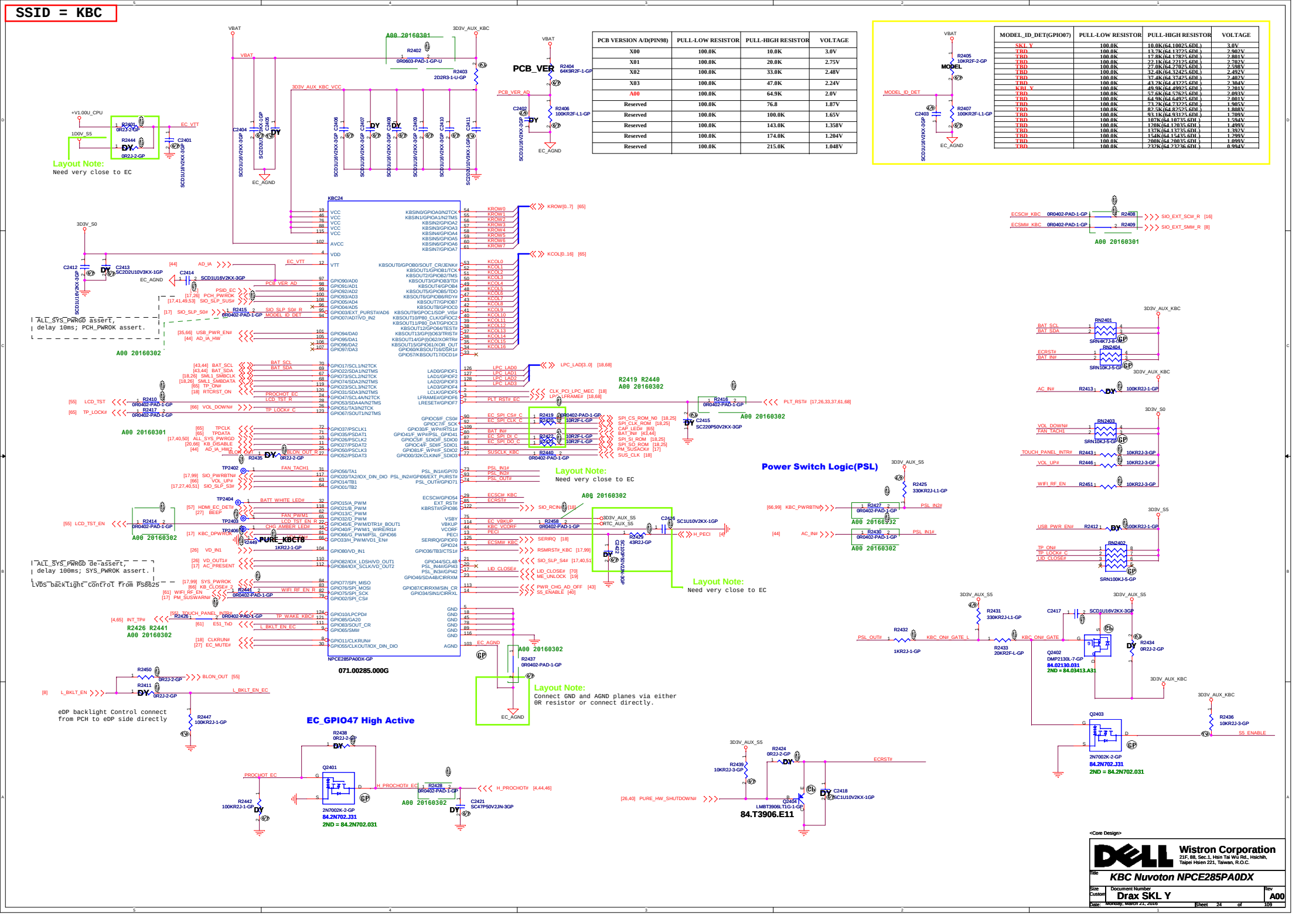
Size	Document Number	Rev
A4	**Drax SKL Y**	**A00**

Date: Thursday, March 17, 2016 Sheet 23 of 109

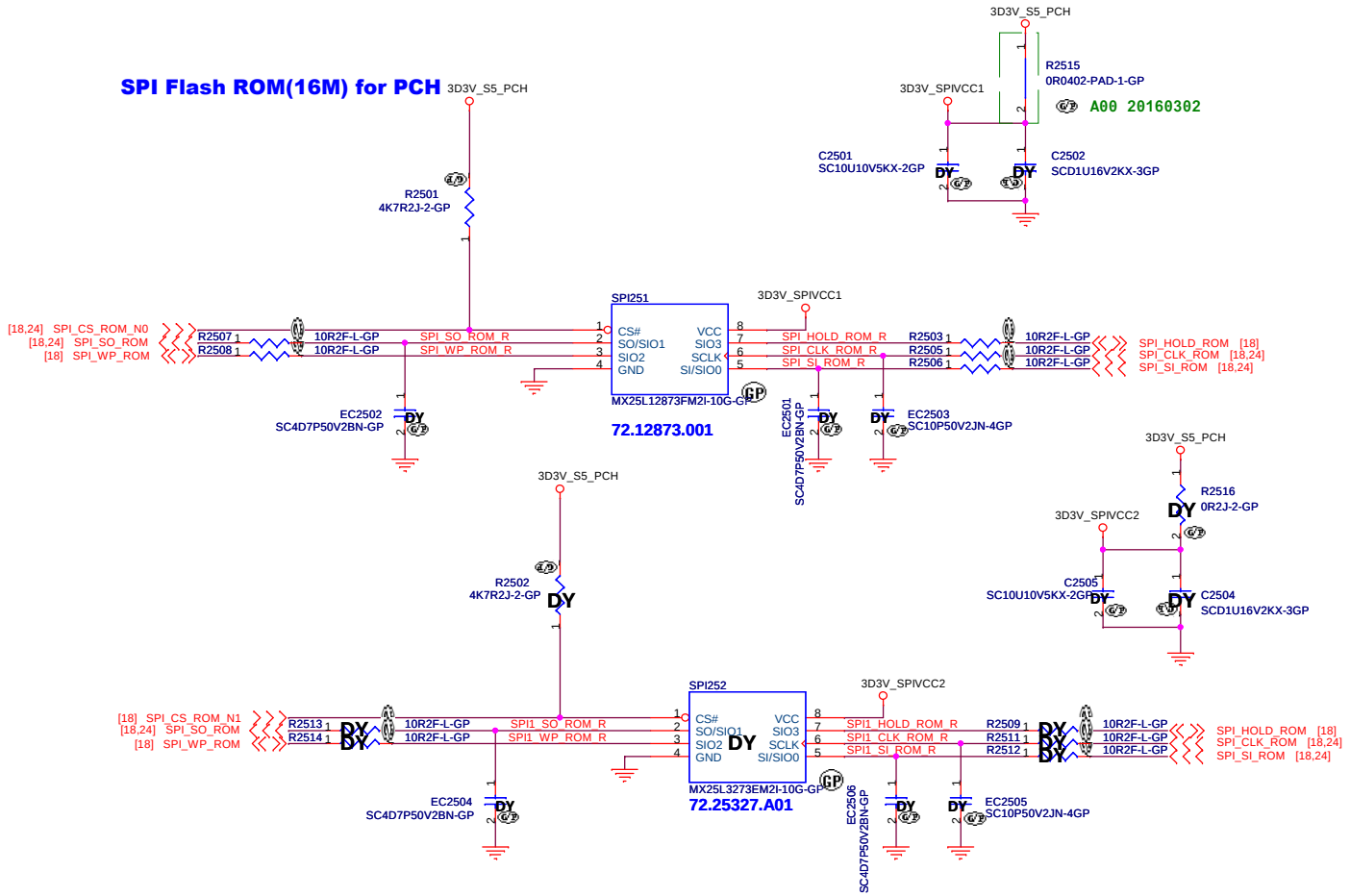
SSID = KBC



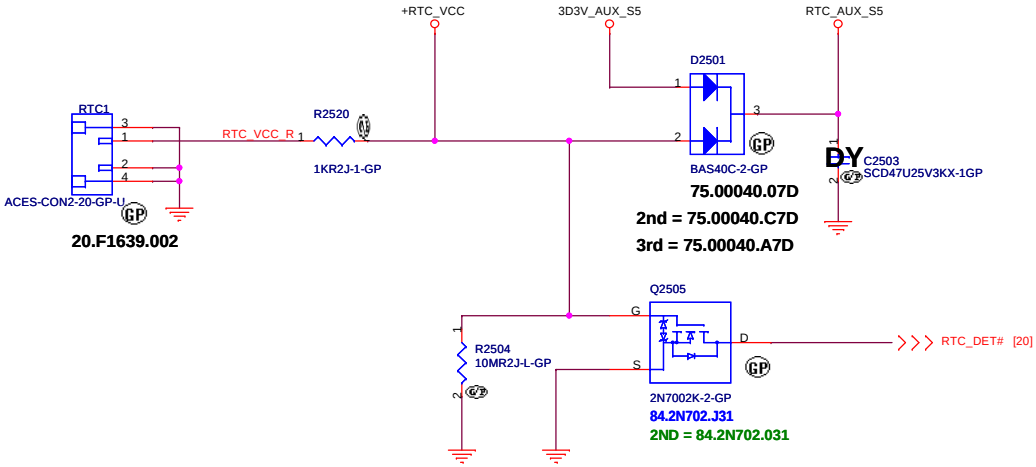
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SKL Y	100.0K	10.0K(64.10025.6DL)	3.0V
TBD	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
TBD	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.407V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
KBL Y	100.0K	49.9K(64.49925.6DL)	2.201V
TBD	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.984V

Main Func = SPI Flash



Main Func = RTC



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Title	Flash/RTC	
Size A3	Document Number Drax SKL Y	Rev A00
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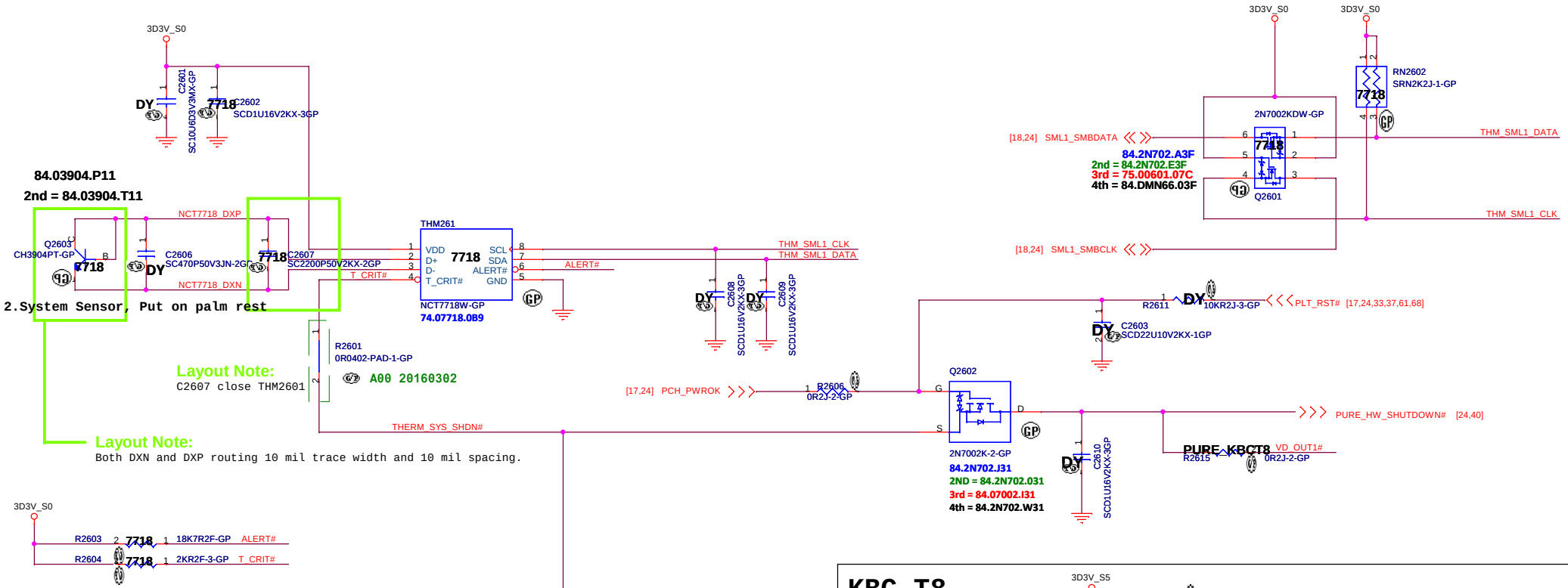
SSID = Thermal Sensor



2.System Sensor, Put on palm rest

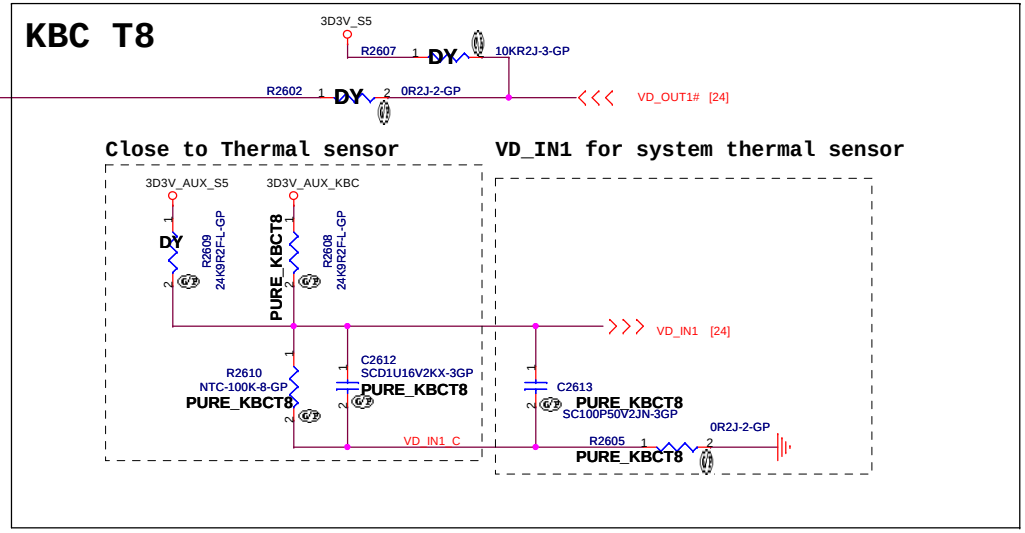
Layout Note:
C2607 close THM2601

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8



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Title: THERMAL NCT7718W/Fan

Size: A3 | Document Number: Drax SKL Y | Rev: A00

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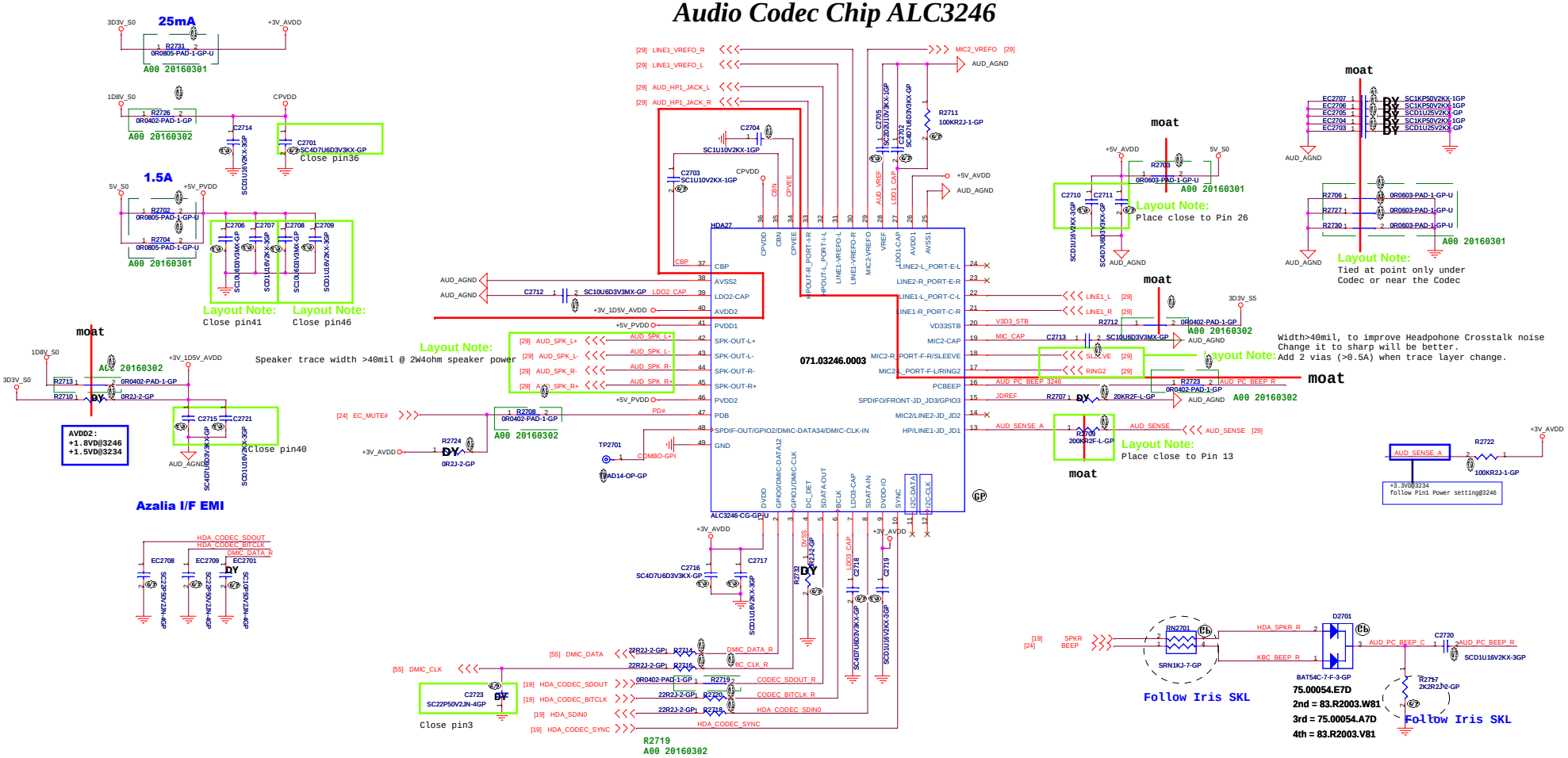
SSID = Audio

Audio Codec Chip ALC3246



+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

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Title: Audio Codec ALC3246

Size: A2 | Document Number: Drax SKL Y | Rev: A00

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Title

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Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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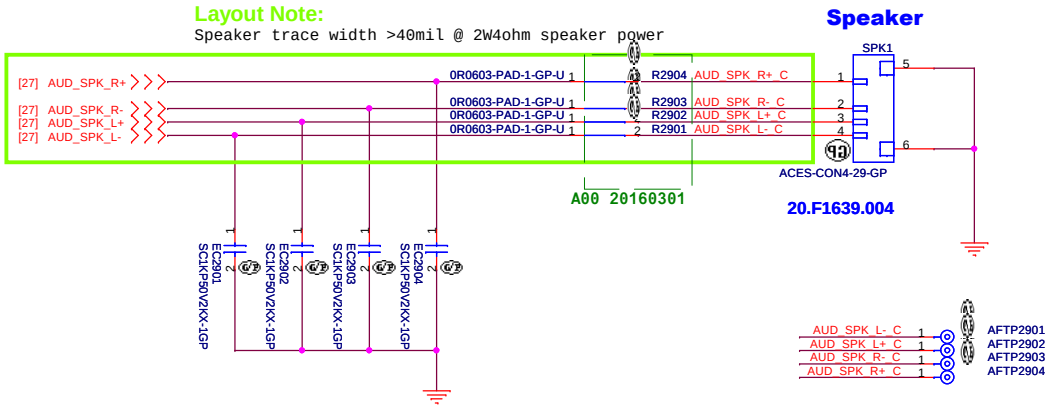
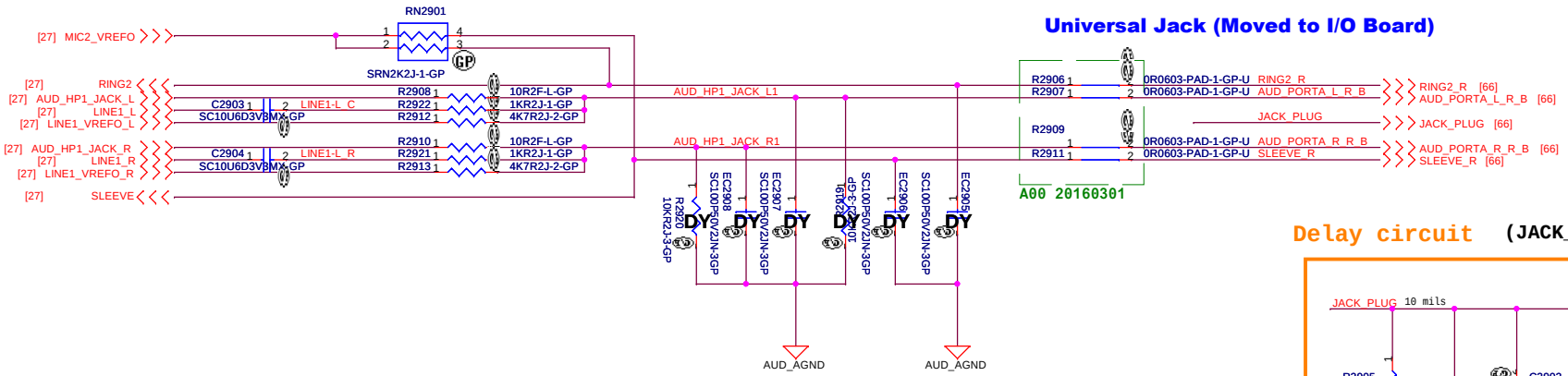
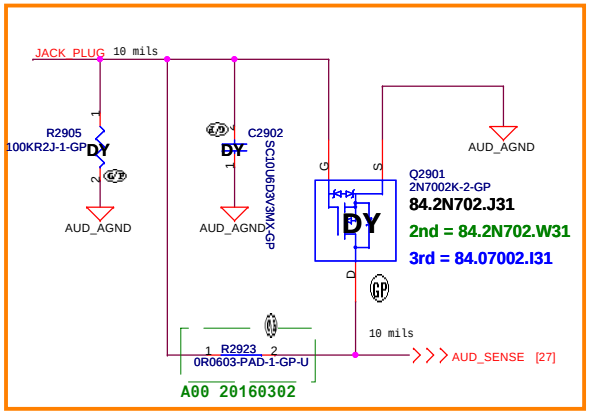
SSID = Audio



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Delay circuit (JACK_PLUG_DET: on IO Board)



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Title: Audio IO

Size: A3 | Document Number: Drax SKL Y | Rev: A00

Date: Monday, March 21, 2016 | Sheet 29 of 109

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Size	Document Number	Rev
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Title: ***(Reserved)***

Size	Document Number	Rev
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Title
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Size	Document Number	Rev
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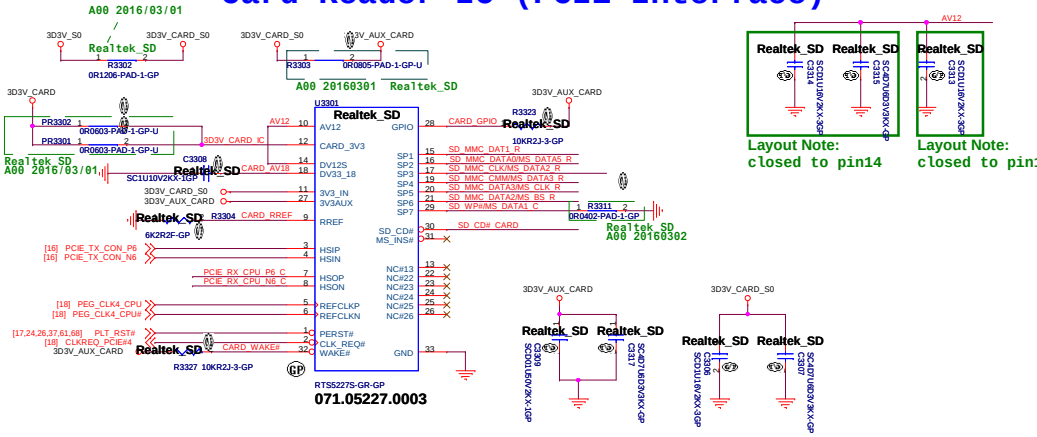
SSID = Card Reader

Card Reader IC (PCIE Interface)

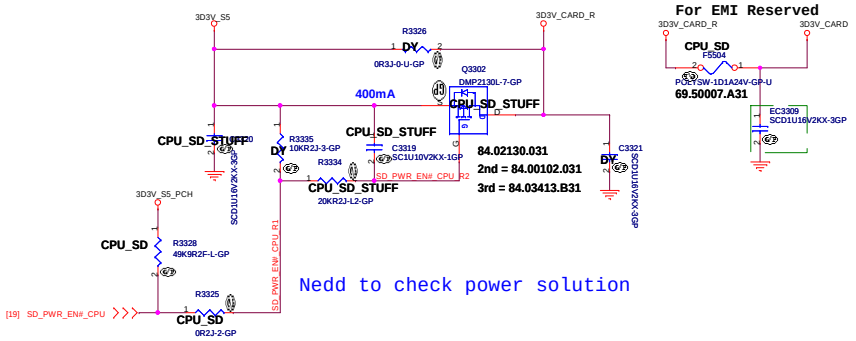


Layout Note:
closed to pin14

Layout Note:
closed to pin10

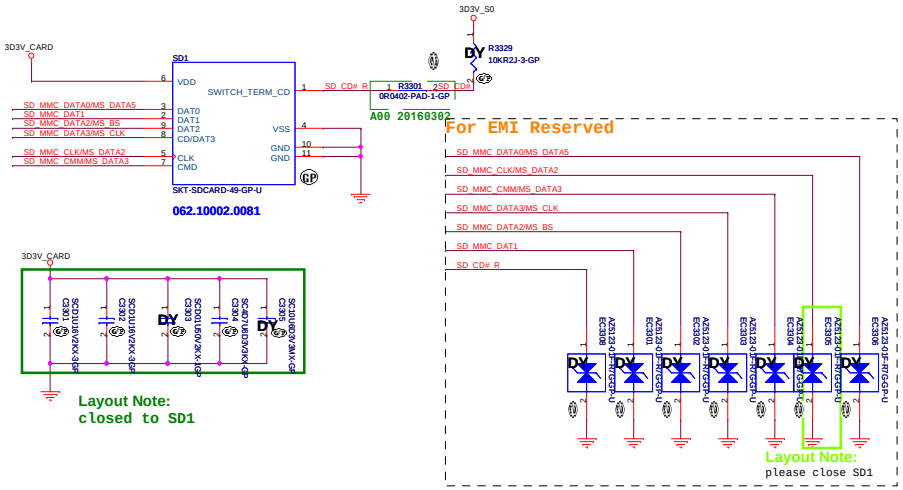
Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD Data 1
SP2	SD_Data_0/MS_Data_1
SP3	SD_Clock_signal/MS_Data_0
SP4	SD_CMD_signal /MS_Data_2
SP5	SD_Data_3/MS_Data_3
SP6	SD_Data_2 /MS_Clock_signal
SP7	SD_WP_signal/MS_BS_signal

Card Reader Power SW (CPU Only)

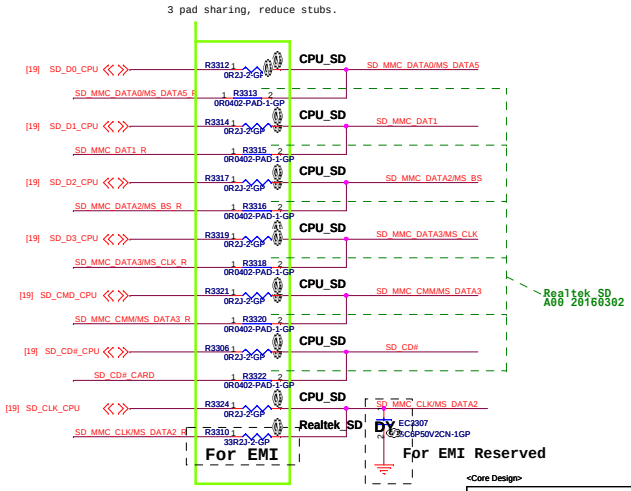


SD Card Connector

Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



Co-lay from CPU and Card Reader IC



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Title: Card Reader + CONN

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 33 of 109

Blanking

<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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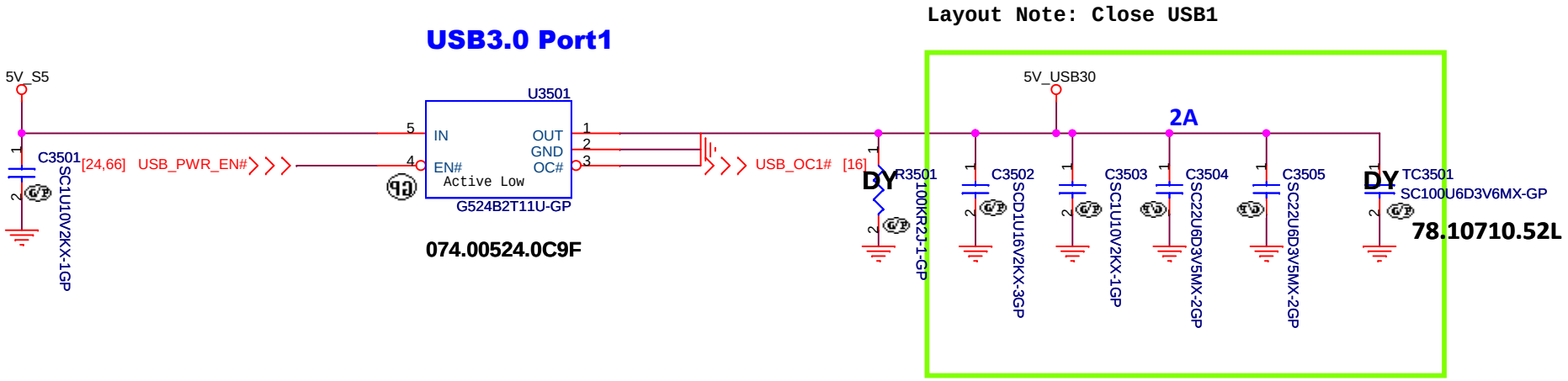
SSID = USB



<Core Design>

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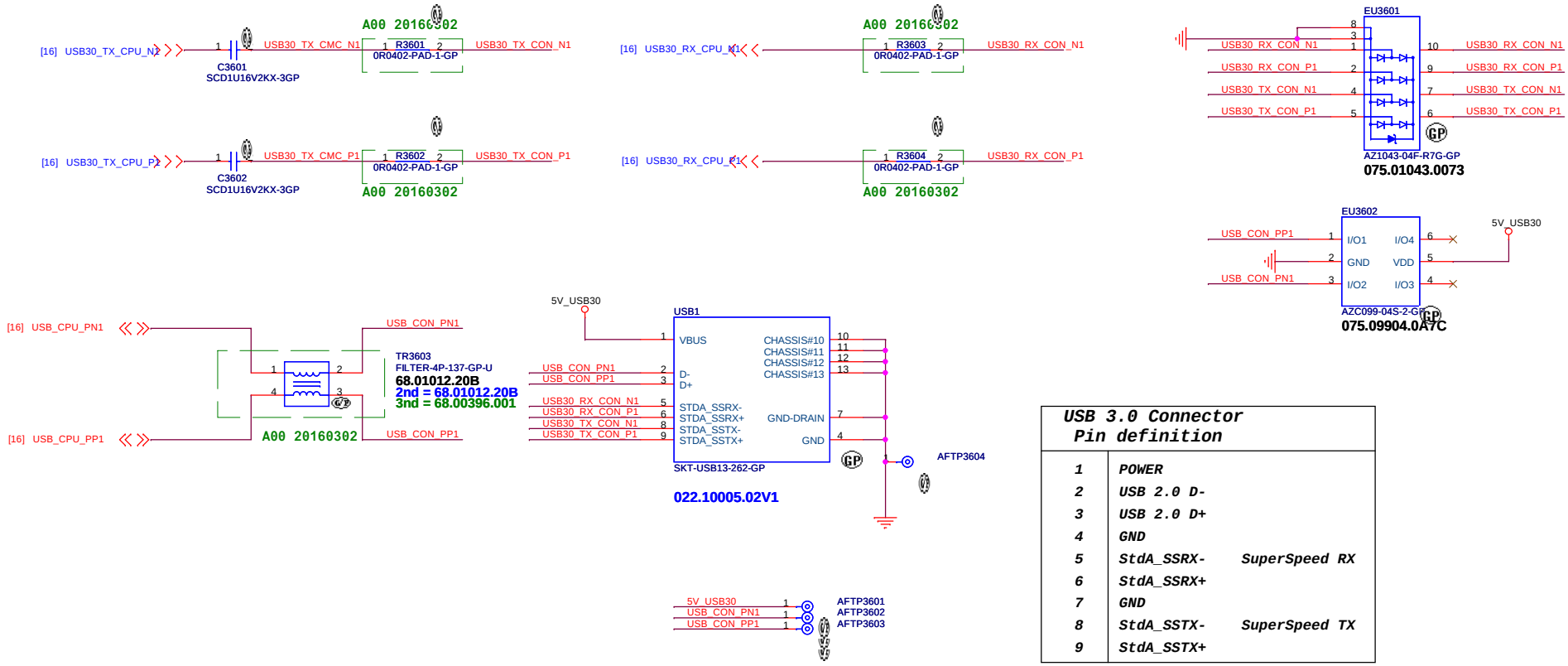
Title	***USB Power SW***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
Date: Monday, March 21, 2016	Sheet 35 of 109	

SSID = USB



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

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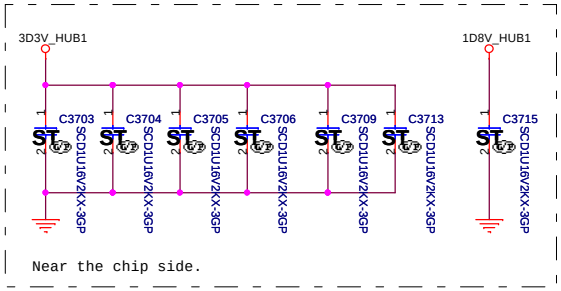
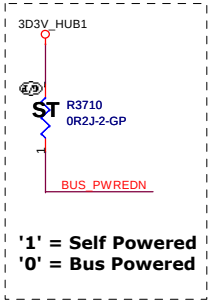
Title: **USB3.0 CONN**

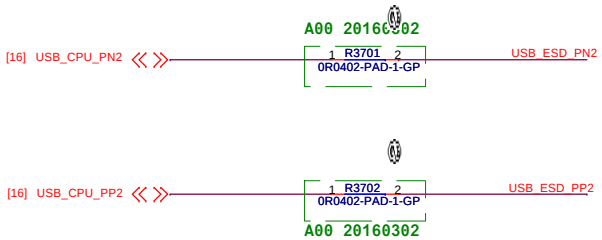
Size | Document Number: **Drax SKL Y** | Rev: **A00**

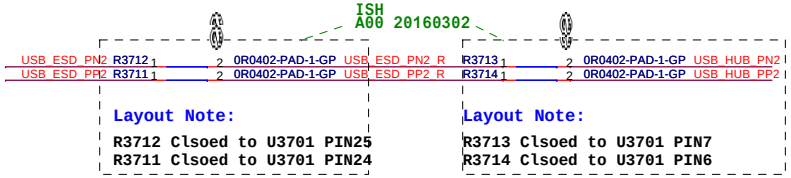
Date: Tuesday, March 22, 2016 | Sheet 36 of 109

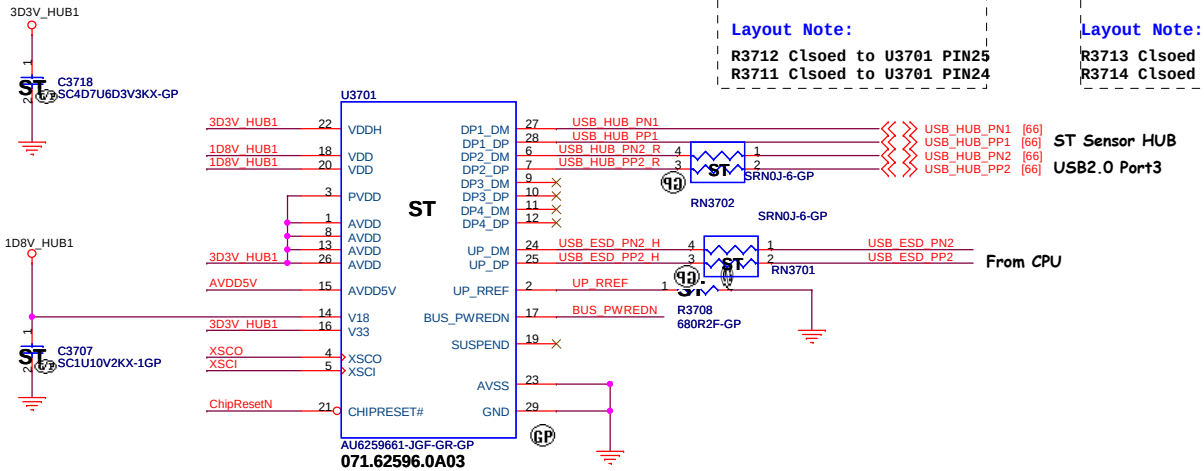
SSID = USB

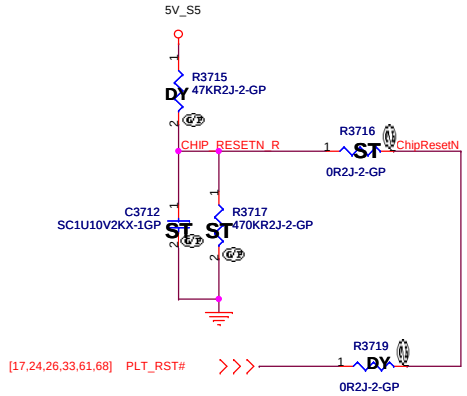


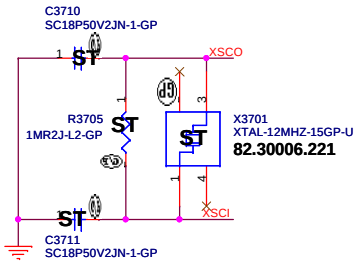


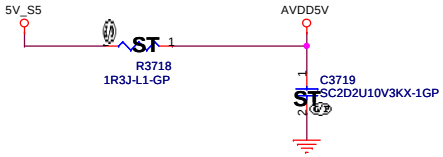












USB Table

Pair	Device
1	USB2.0 Port3
2	Sensor HUB
3	
4	

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Title: USB2.0 HUB

Size: A3 | Document Number: Drax SKL Y | Rev: A00

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Title

(Reserved)

Size	Document Number	Rev
A4	Drax SKL Y	A00

Blanking

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Title

(Reserved)

Size	Document Number	Rev
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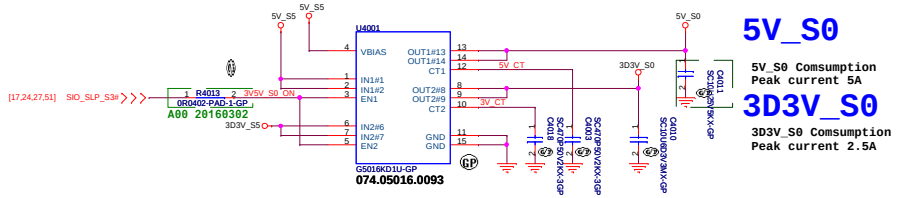
SSID= Power Plane & Sequence

ROSA Run Power



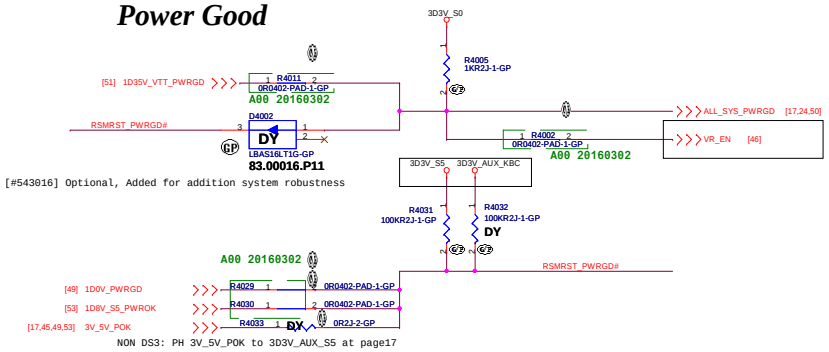
5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

Power Good

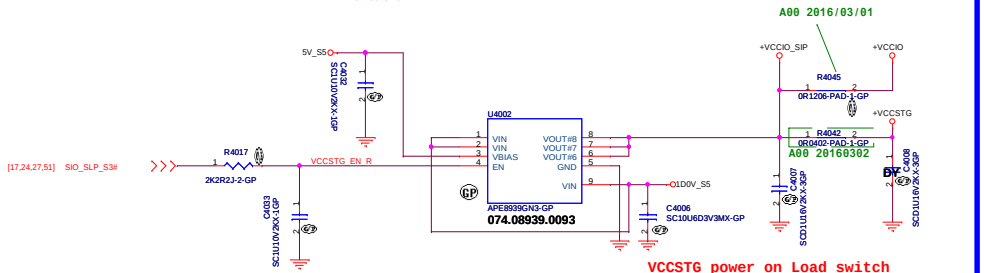


[#543016] Optional, Added for addition system robustness

NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

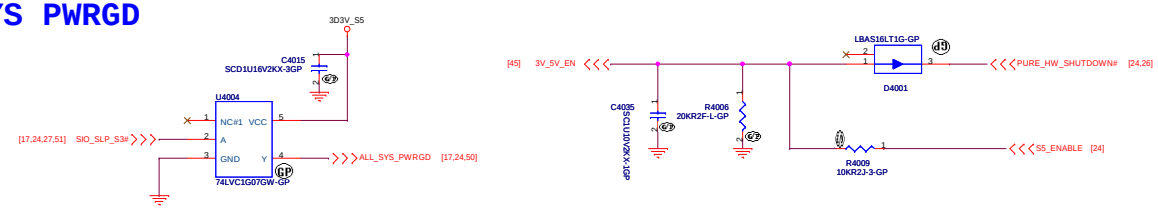
VCCIO and VCCSTG

Modify power switch IC and relate schematic
DVT2 2016/01/21



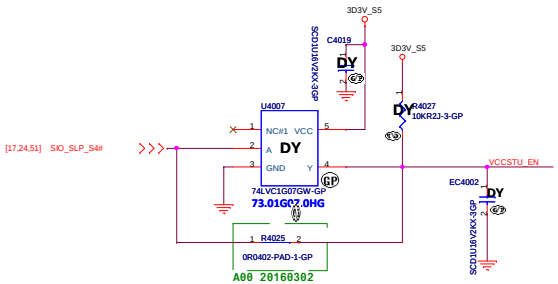
VCCSTG power on Load switch
SLEW RATE=10US < TR < 65US

ALL SYS PWRGD

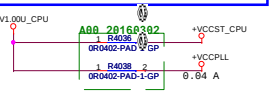


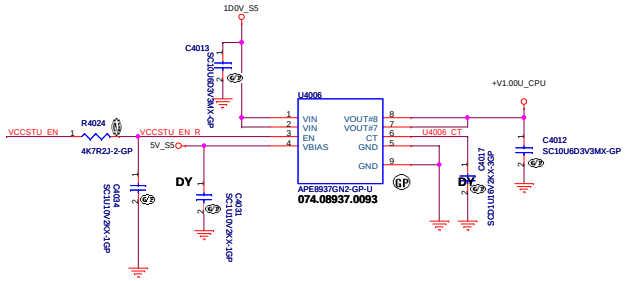
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.



VCCST





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Title: Power Plane Enable
Size: A2
Document Number: Drax SKL Y
Rev: A00
Date: Tuesday, March 22, 2016
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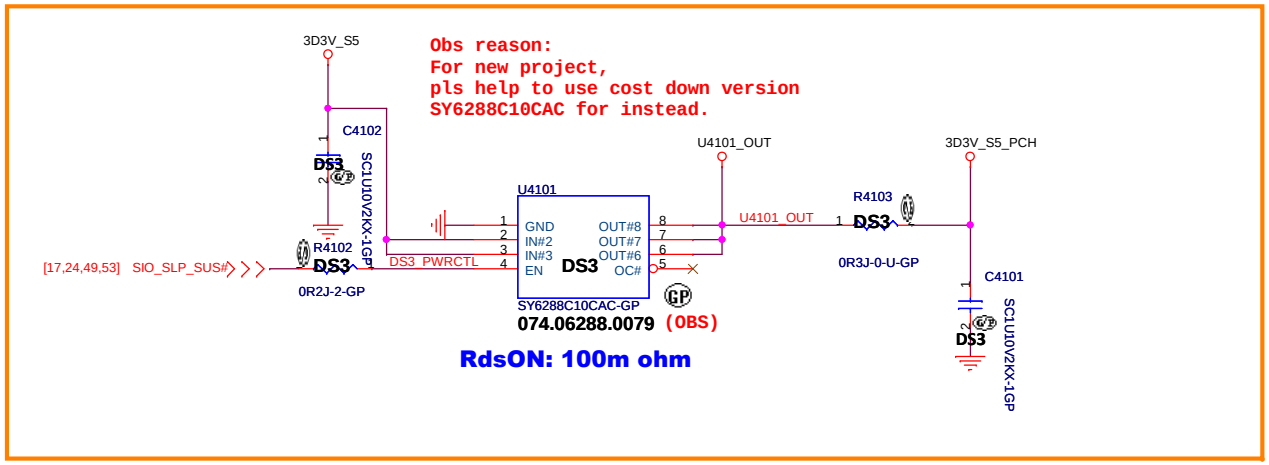
SSID = DS3



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Title	*DS3*	
Size B	Document Number **Drax SKL Y**	Rev **A00**
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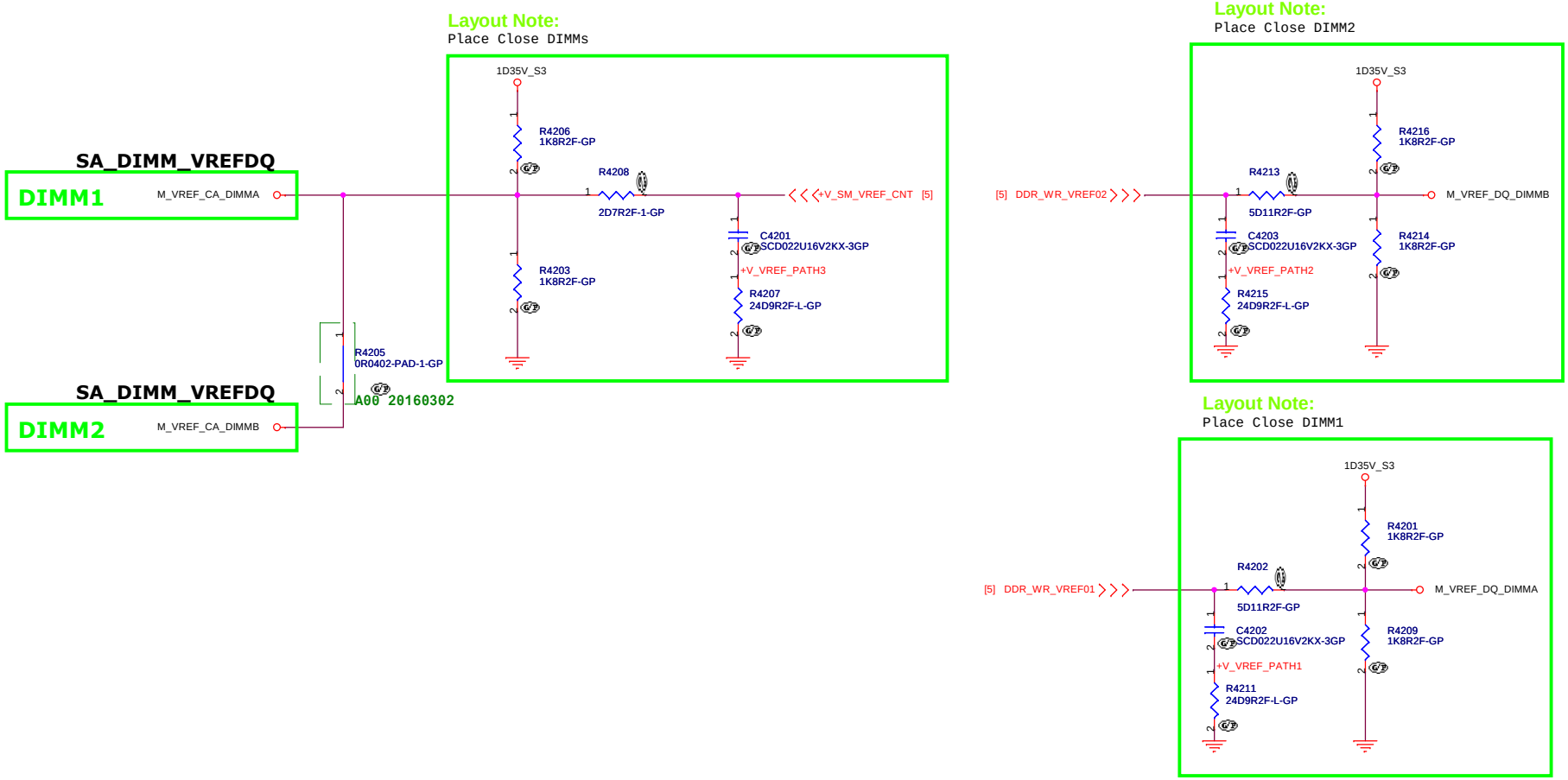
SSID = DIMM1

VREF CIRCUITRY



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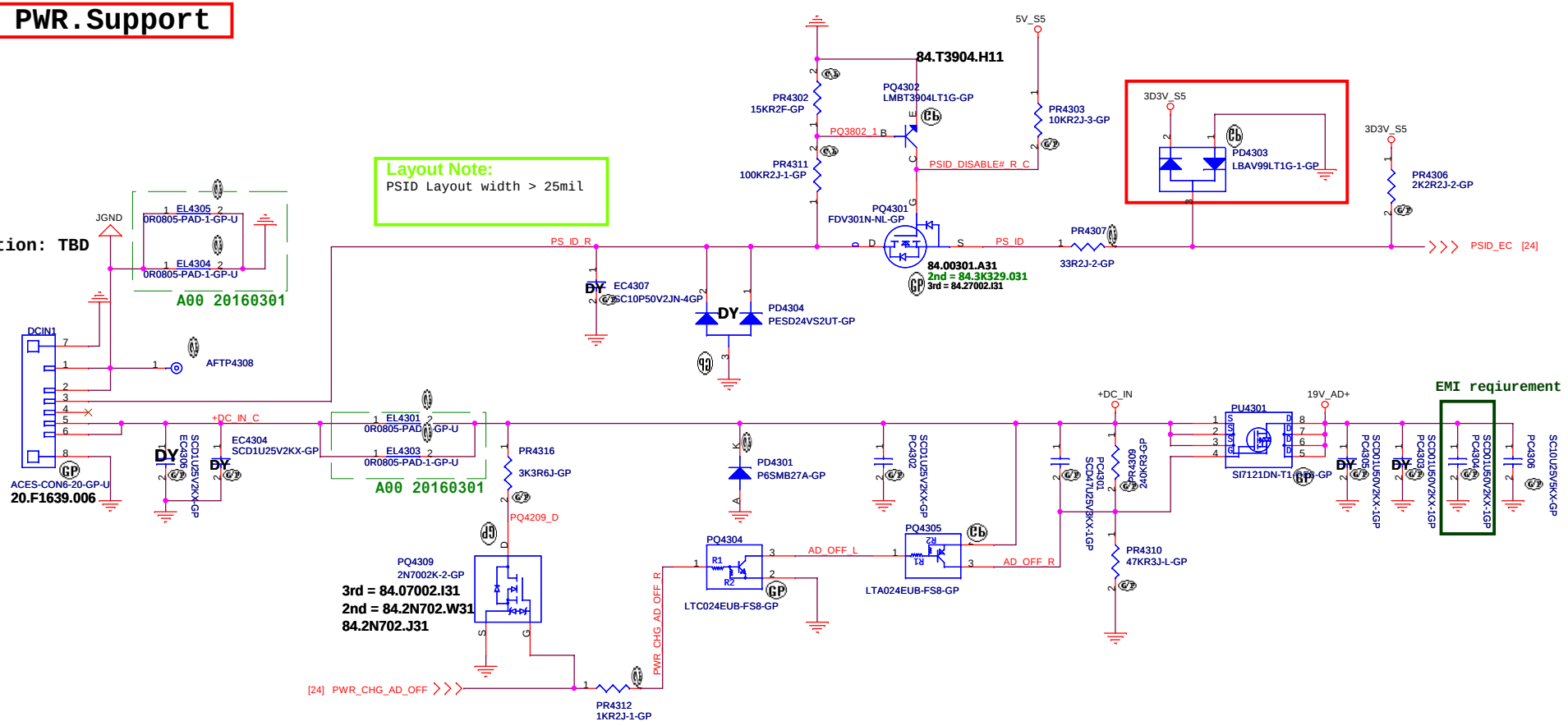
Title	DIMM1 POWER	
Size A3	Document Number Drax SKL Y	Rev A00
Date: Monday, March 21, 2016	Sheet 42 of 109	

SSID = PWR.Support

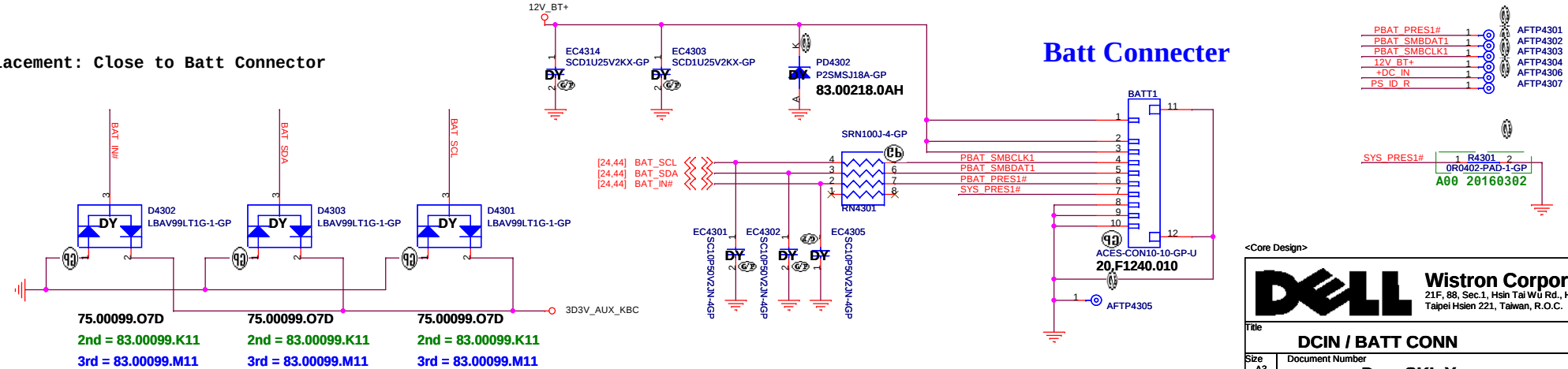
Pin Definition: TBD

Layout Note:
PSID Layout width > 25mil



SSID = PWR.Support

Placement: Close to Batt Connector



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Title	DCIN / BATT CONN	
Size A3	Document Number Drax SKL Y	Rev A00
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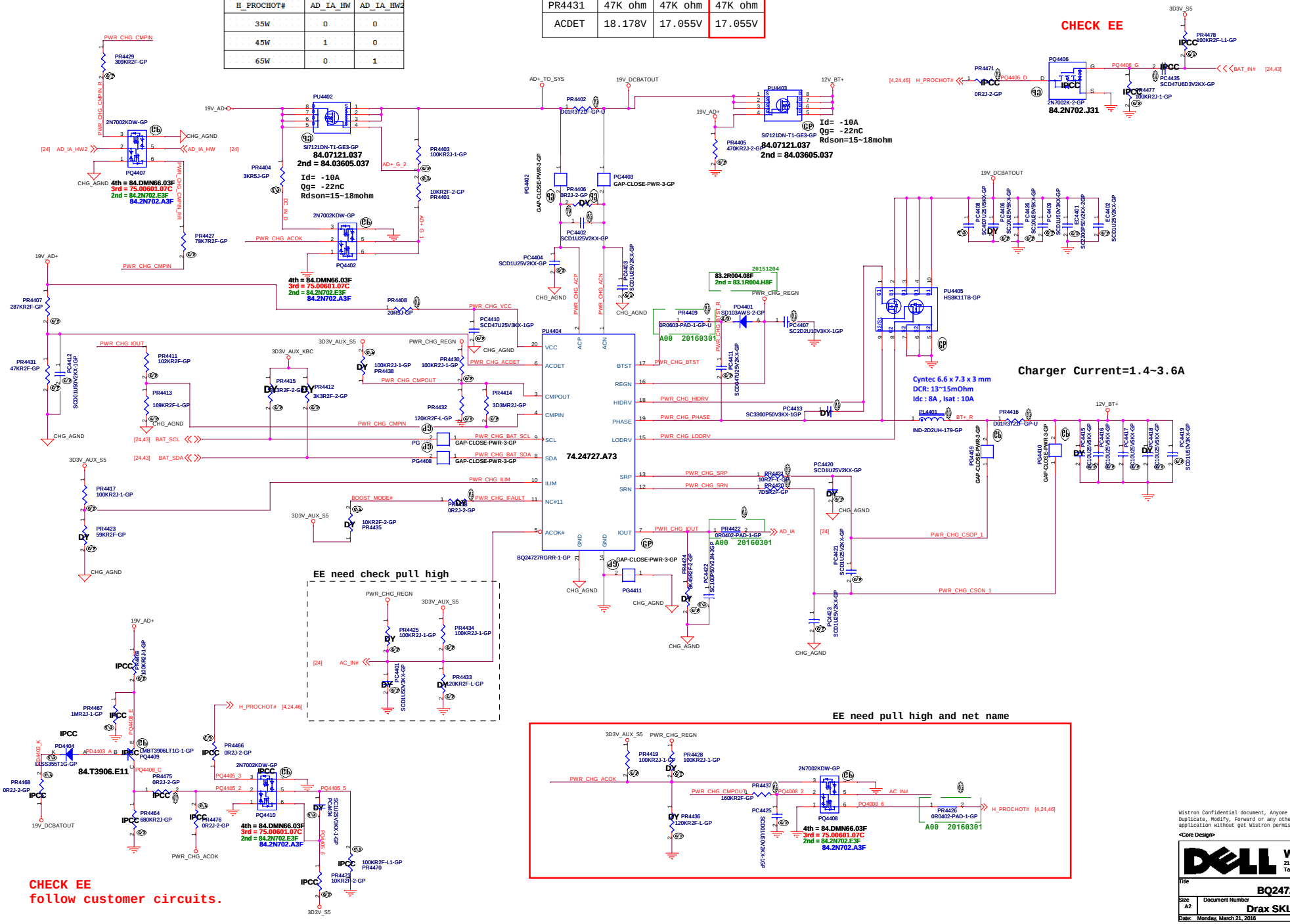
SSID = Charger

BT Cell	4 Cells	3 Cells	2 Cells
PR4407	309K ohm	287K ohm	287K ohm
PR4431	47K ohm	47K ohm	47K ohm
ACDET	18.178V	17.055V	17.055V

EC code only BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1



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Title: BQ24727_CHARGER

Size: A2 | Document Number: Drax SKL Y | Rev: A00

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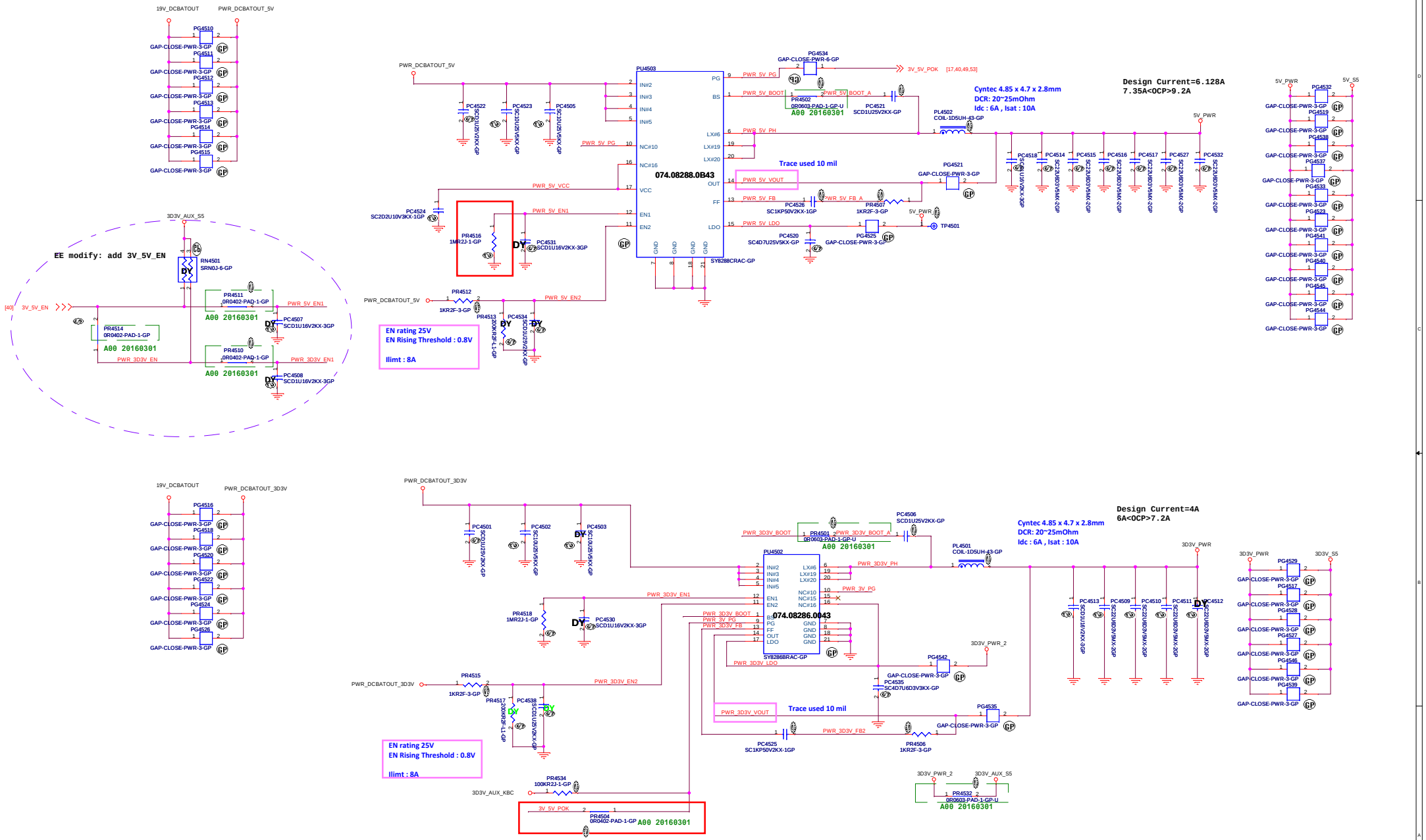
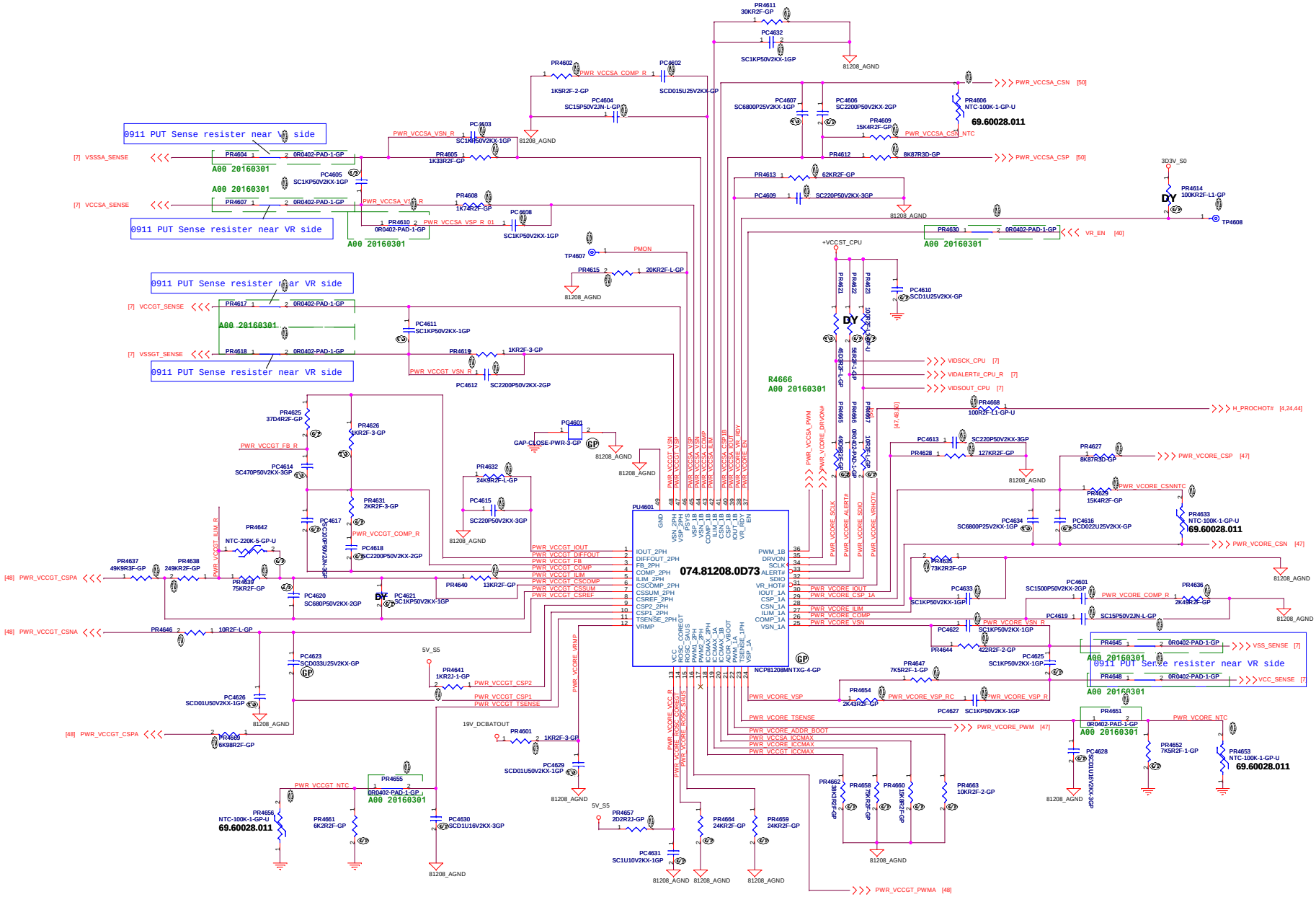
SSID = Charger



Main Func = CPU_CORE



<Core Design>

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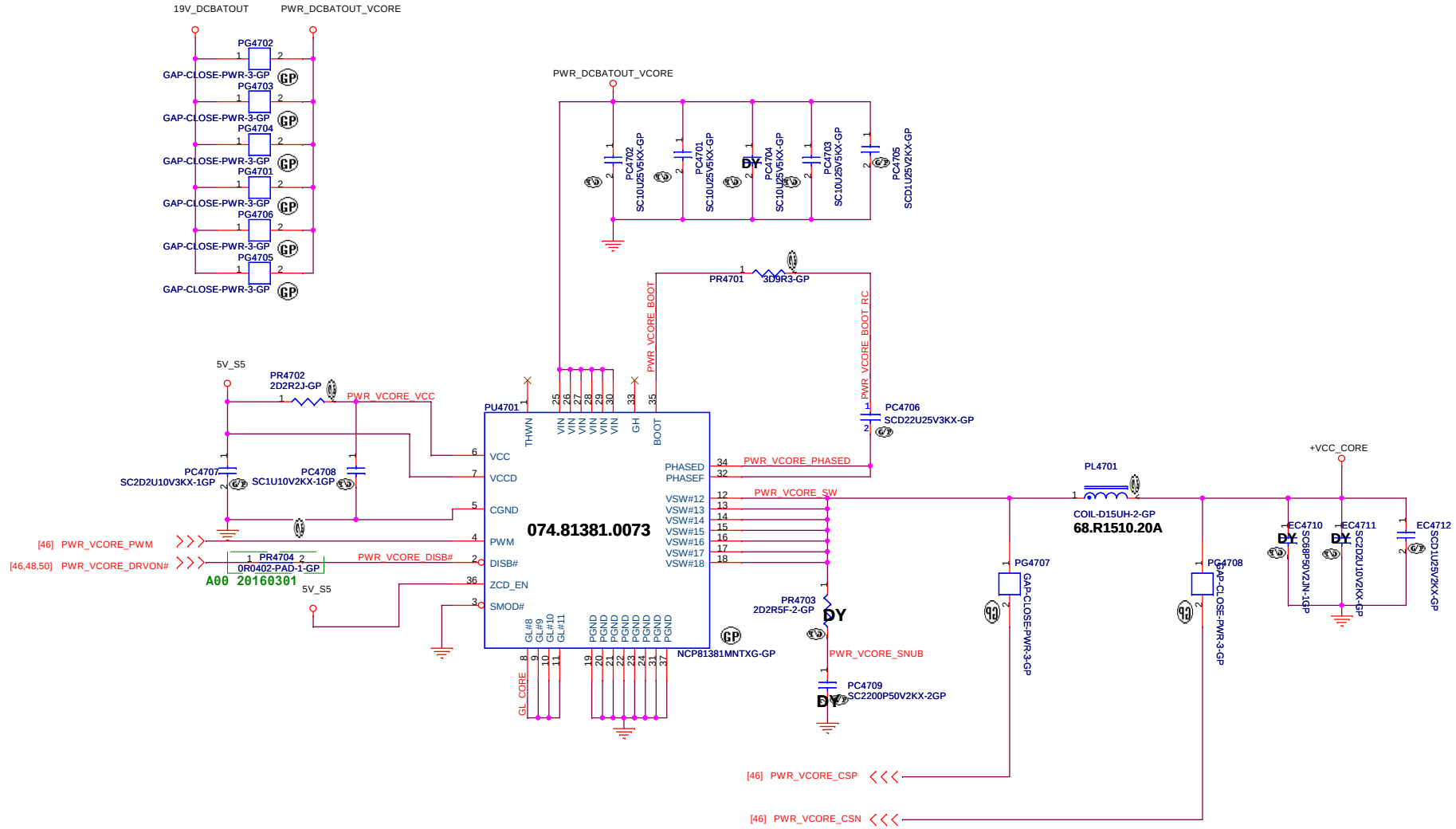
Title: NCP81201MNTXG_CPUCORE(1/3)

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 46 of 109

Main Func = CPU_CORE



<Core Design>

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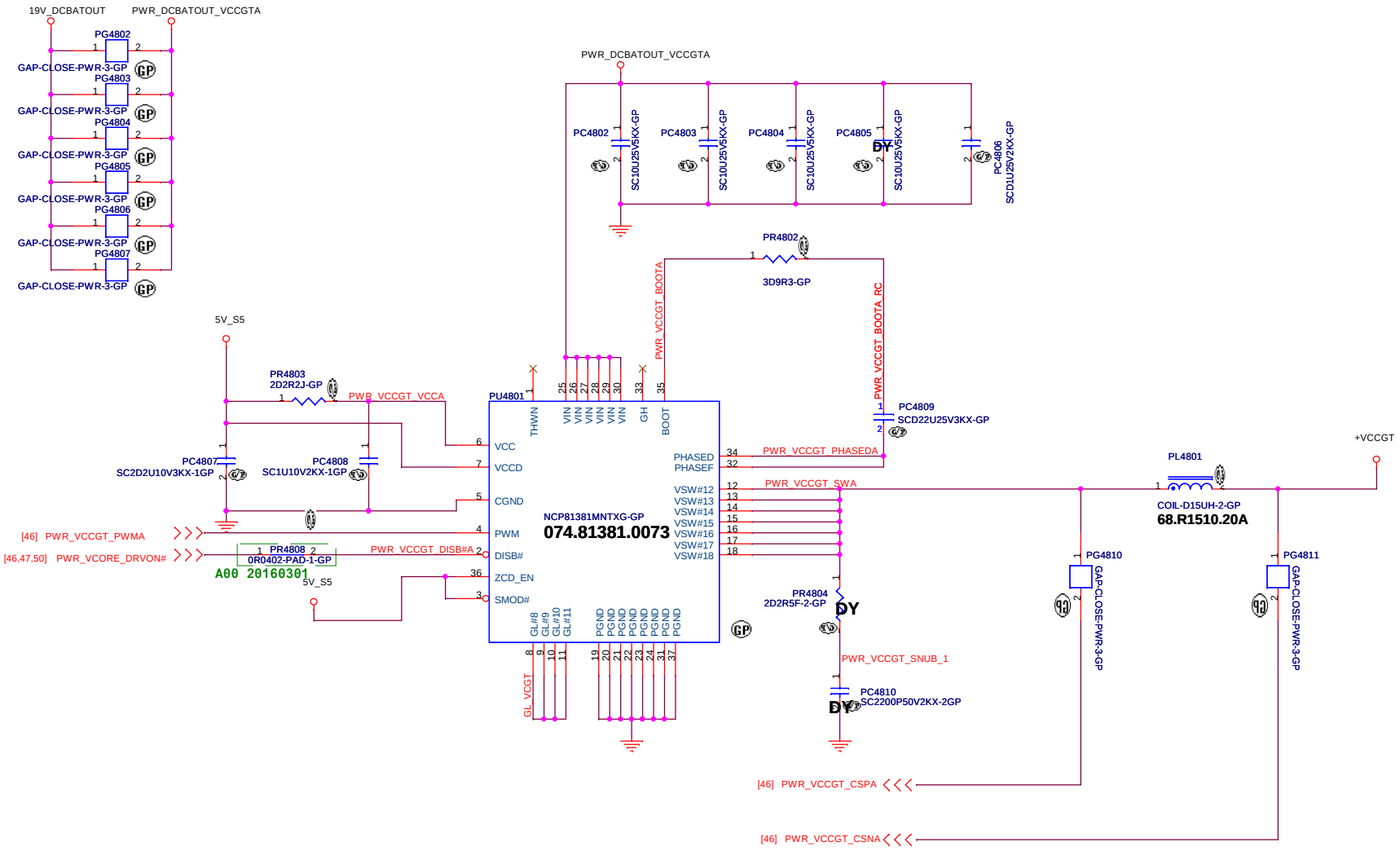
Title: *NCP81201MNTXG CPUCORE(2/3)*

Size: A3 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 47 of 109

Main Func = CPU_CORE



<Core Design>

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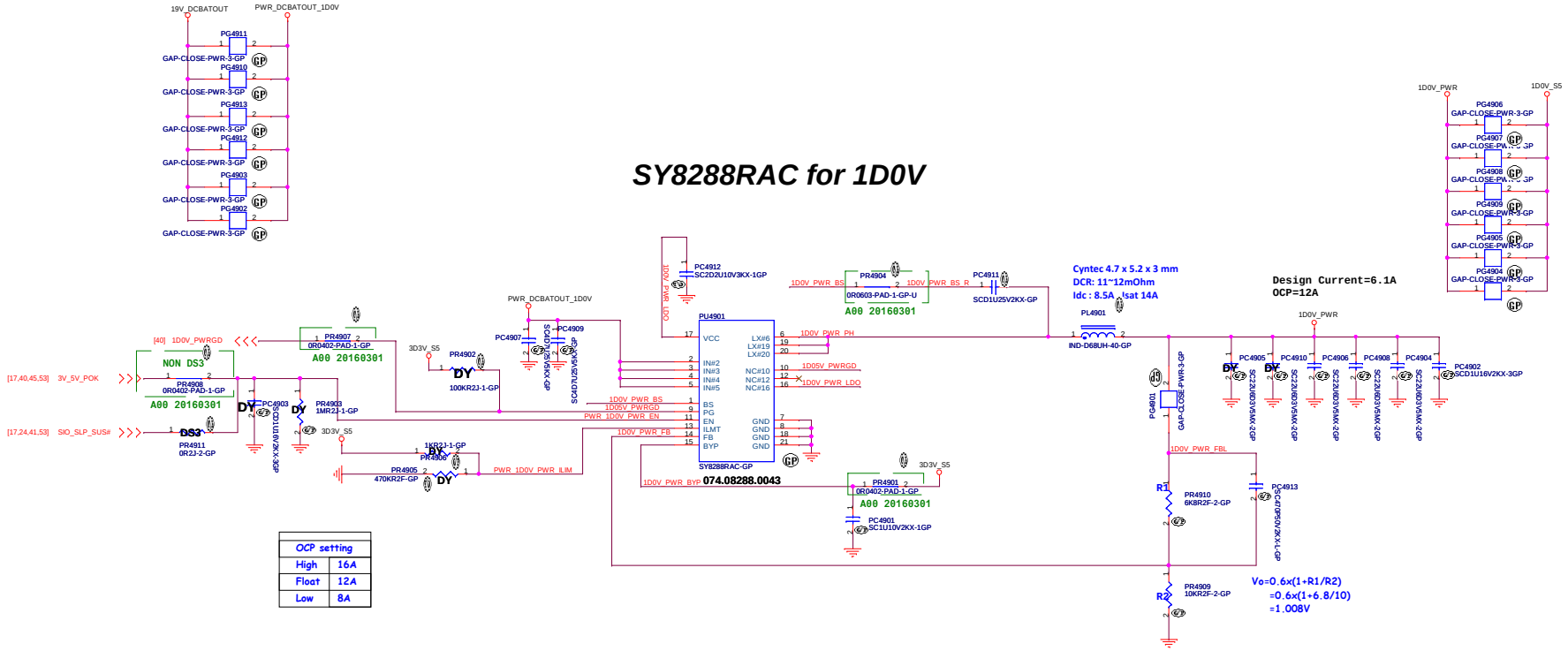
Title	NCP81201MNTXG_GFXCORE(3/3)	
Size A3	Document Number Drax SKL Y	Rev A00
Date: Thursday, March 17, 2016	Sheet 48 of 109	

SSID = PWR.Plane.Regulator_1p0v

SY8288RAC for 1D0V



OCP setting	
High	16A
Float	12A
Low	8A

<Core Design>

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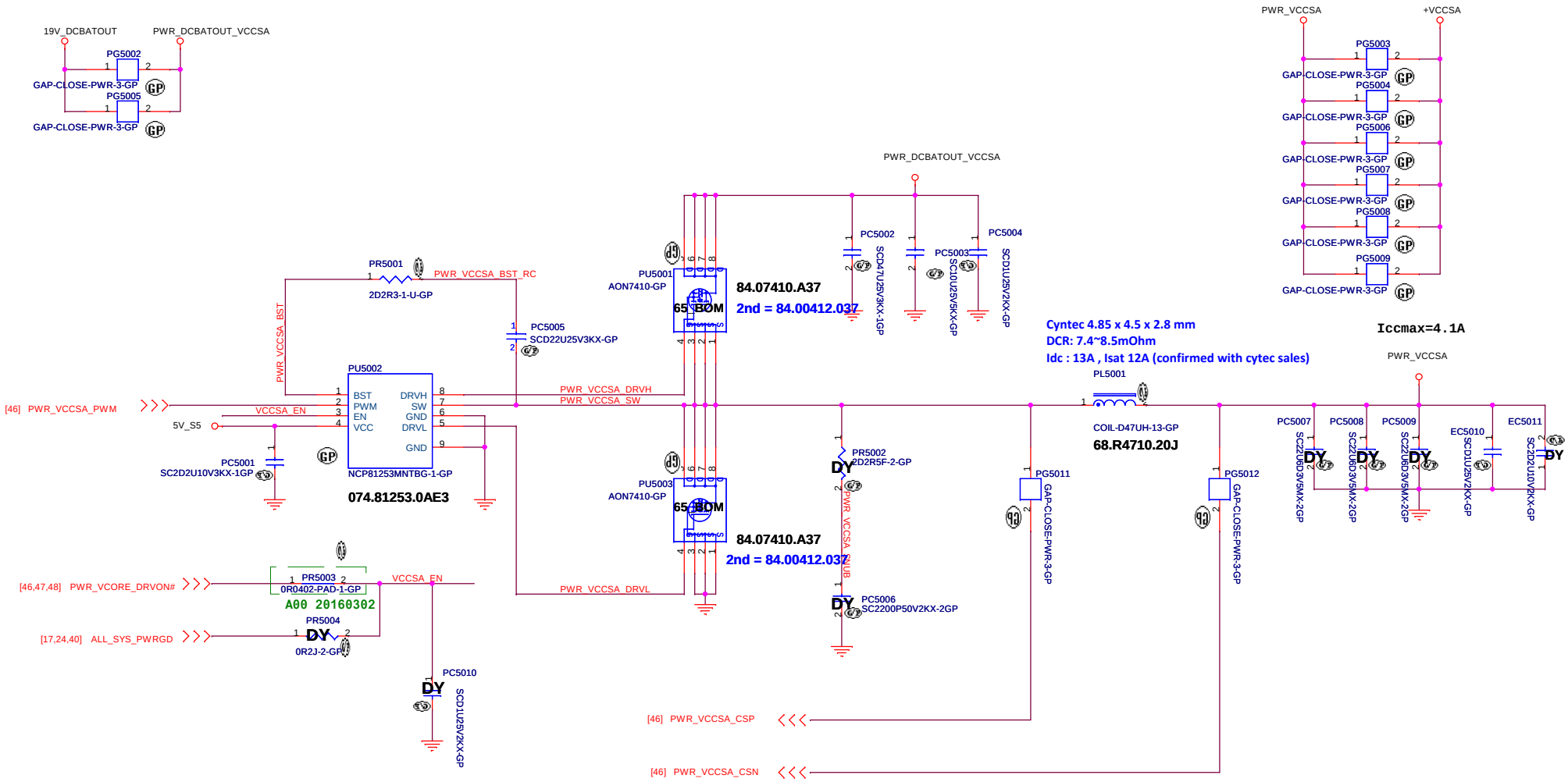
Title: SY8288_1D0V

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 49 of 109

Main Func = CPU_CORE



<Core Design>

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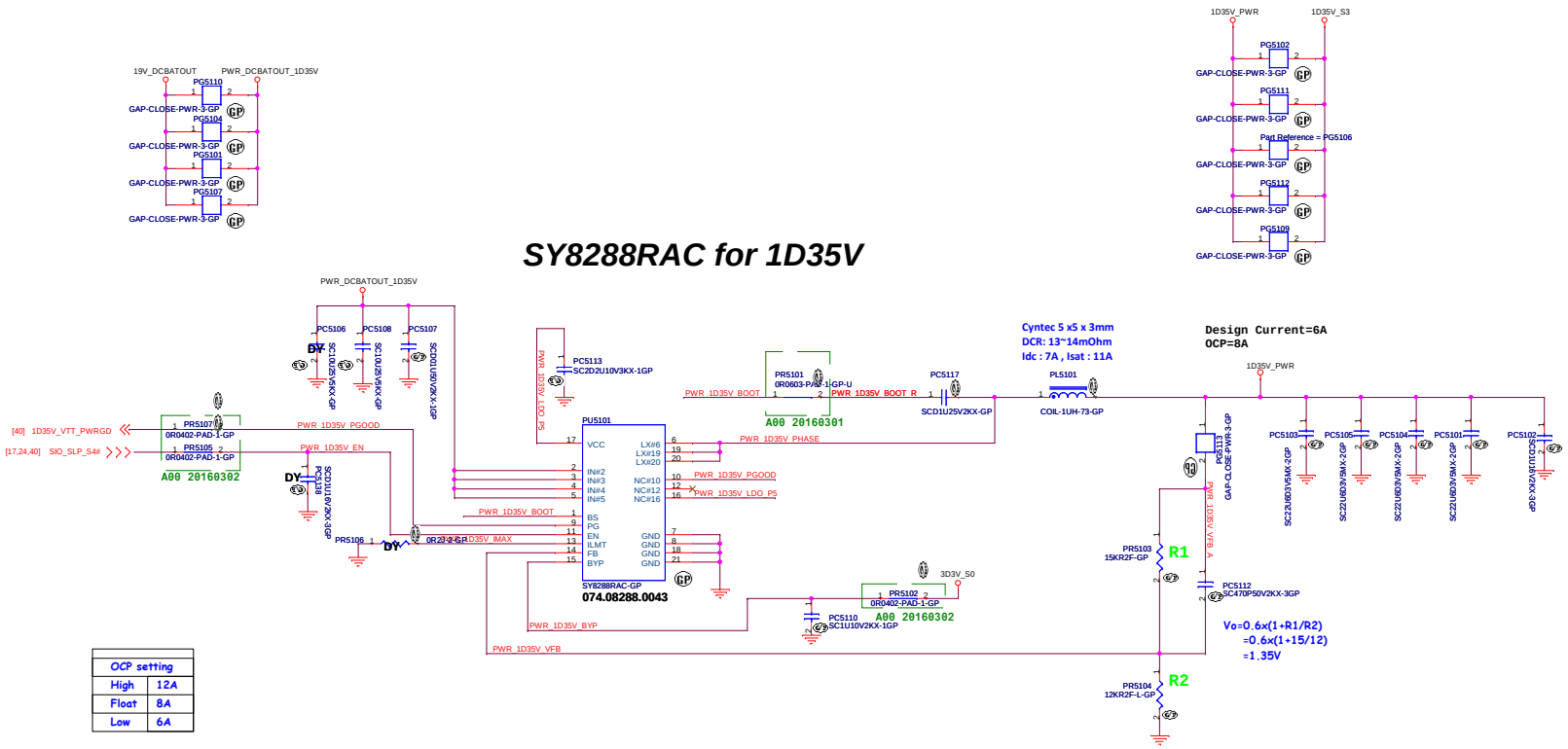
Title: ***NCP81253MN_CPU_VCCSA***

Size	Document Number	Rev
A3	*Drax SKL Y*	*A00*

Date: Tuesday, March 22, 2016 Sheet 50 of 109

SSID = PWR.Plane.Regulator_1p2v



<Core Design>

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Title: SY8288_1D35V/APL5338_0D675V

Size: A2 | Document Number: Drax SKL Y | Rev: A00

Date: Thursday, March 17, 2016 | Sheet 51 of 109

Blanking

<Core Design>

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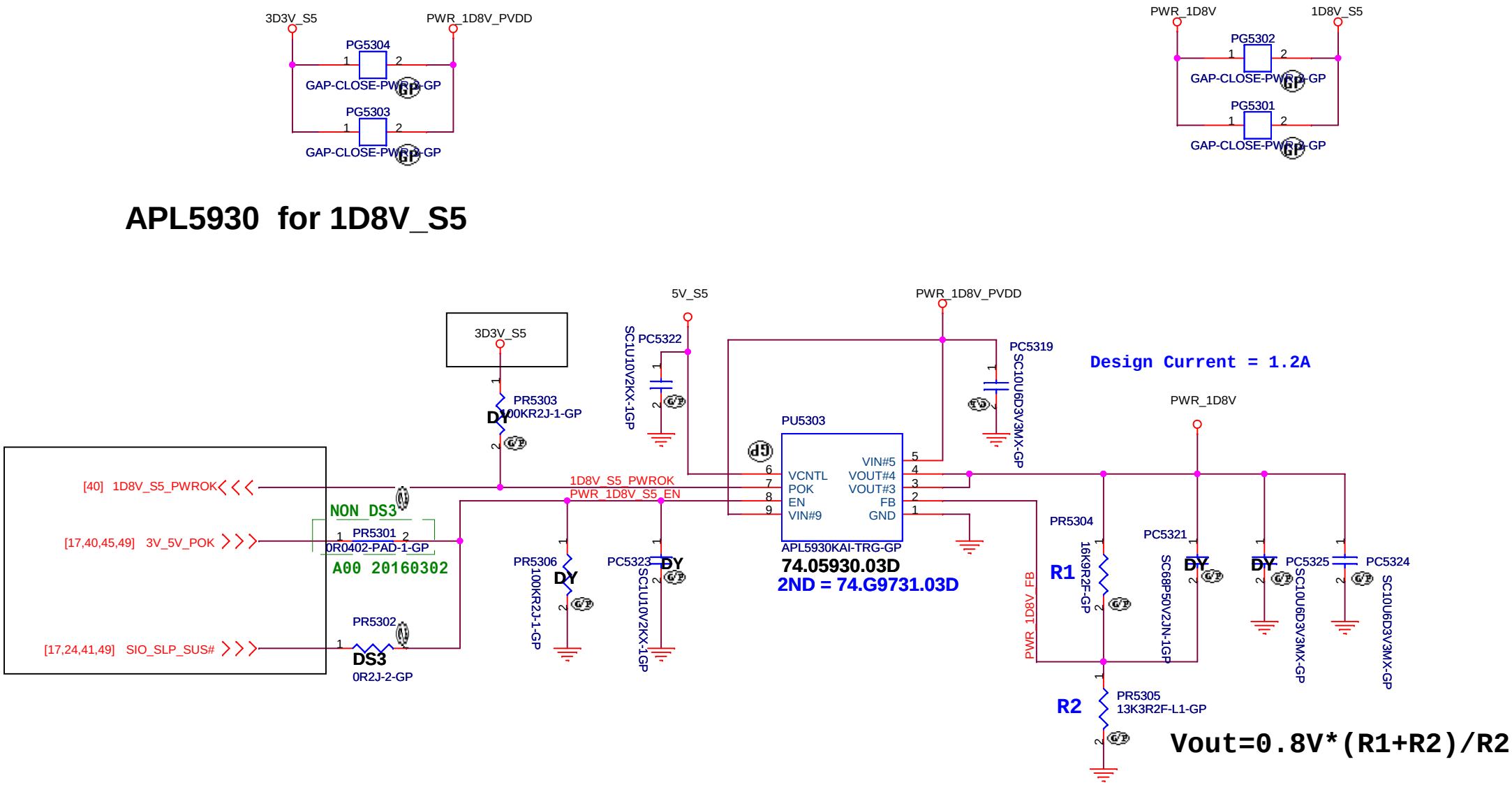
Title	***S1339D15_1D5V***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
Date: Thursday, March 17, 2016	Sheet 52 of 109	

SSID = PWR.Plane.Regulator_1p8v



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Title: ***SYW232_1D8V***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

Date: Tuesday, March 22, 2016 Sheet 53 of 109

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<Core Design>

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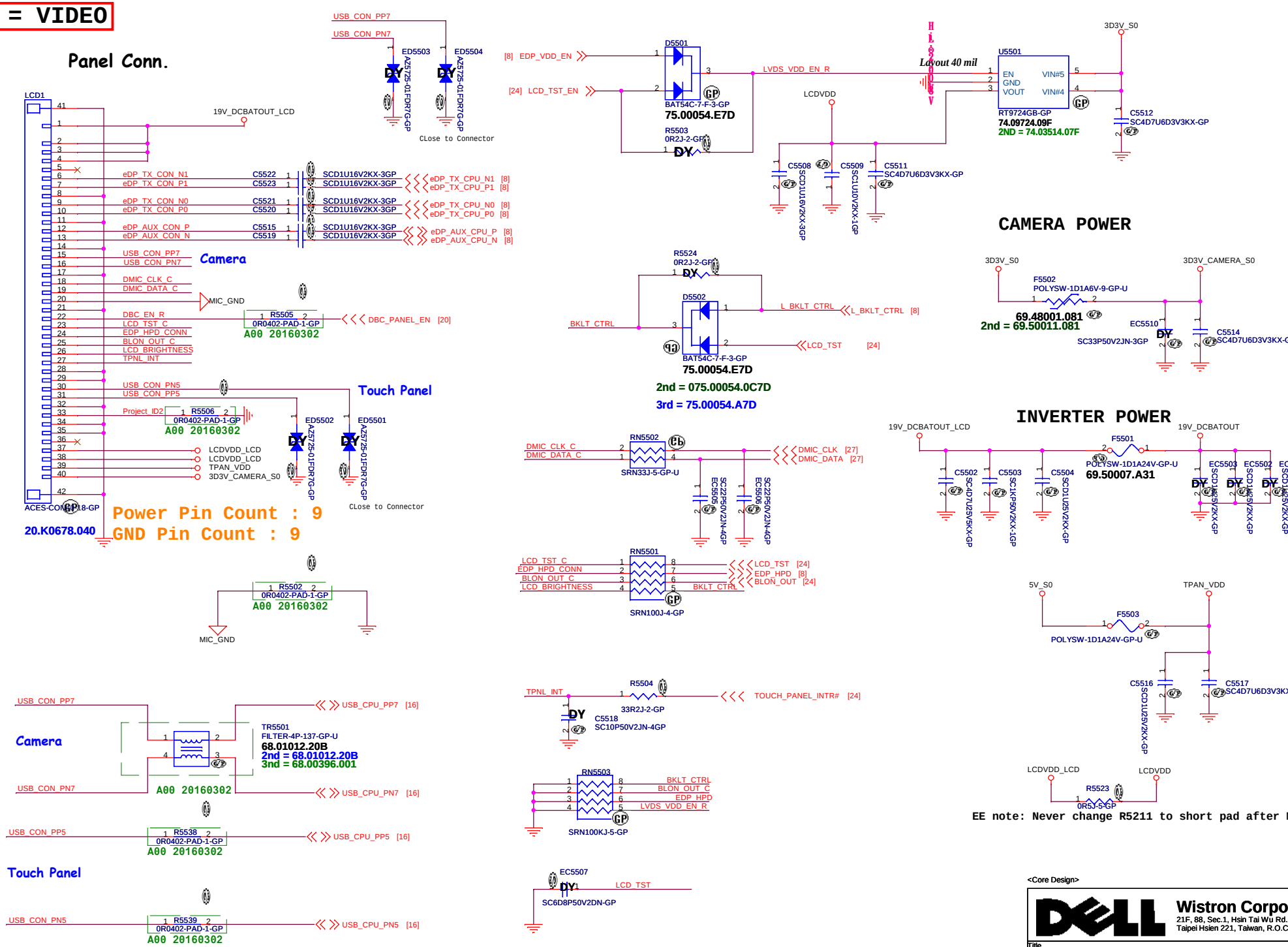
Title

APL5930_1D24V

Size	Document Number	Rev
A4	**Drax SKL Y**	A00

SSID = VIDEO

Panel Conn.



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<Core Design>

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 55 of 109

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Title

(Reserved)

Size	Document Number	Rev
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SSID = VIDEO

[8] HDMI_CLK#
[8] HDMI_CLK
[8] HDMI_DATA0#
[8] HDMI_DATA0
[8] HDMI_DATA1#
[8] HDMI_DATA1
[8] HDMI_DATA2#
[8] HDMI_DATA2

C5709 1 — SCD1U16V2KX-3GP — HDMI_CLK# R
C5706 1 — SCD1U16V2KX-3GP — HDMI_CLK R
C5702 1 — SCD1U16V2KX-3GP — HDMI_DATA0# R
C5701 1 — SCD1U16V2KX-3GP — HDMI_DATA0 R
C5704 1 — SCD1U16V2KX-3GP — HDMI_DATA1# R
C5708 1 — SCD1U16V2KX-3GP — HDMI_DATA1 R
C5707 1 — SCD1U16V2KX-3GP — HDMI_DATA2# R
C5705 1 — SCD1U16V2KX-3GP — HDMI_DATA2 R

RN5701 SRN470J-3-GP
RN5703 SRN470J-3-GP

HDMI_PLL_GND

R5706 0R2J-2-GP DY

Q5703 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31

5V_S0

R5703 DY 100KR2J-1-GP

5V_S0

D5701 LBAW56LT1G-GP
83.00056.Y11

DDC_CLK_PH1
DDC_DATA_PH2

RN5702 SRN2K2J-1-GP

3D3V_S0

Q5701 2N7002KDW-GP

[8] CPU_DP1_CTRL_CLK
[8] CPU_DP1_CTRL_DATA

DDC_CLK_HDMI
DDC_DATA_HDMI

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

HDMI_CLK# R — R5714 0R0402-PAD-1-GP — HDMI_CLK# R_C
A00 20160302

R5710 150R2J-L1-GP-U

HDMI_CLK R — R5715 0R0402-PAD-1-GP — HDMI_CLK R_C
A00 20160302

HDMI_DATA2# R — R5716 0R0402-PAD-1-GP — HDMI_DATA2# R_C
A00 20160302

R5704 150R2J-L1-GP-U

HDMI_DATA2 R — R5717 0R0402-PAD-1-GP — HDMI_DATA2 R_C
A00 20160302

HDMI_DATA0# R — R5721 0R0402-PAD-1-GP — HDMI_DATA0# R_C
A00 20160302

R5709 150R2J-L1-GP-U

HDMI_DATA0 R — R5720 0R0402-PAD-1-GP — HDMI_DATA0 R_C
A00 20160302

HDMI_DATA1# R — R5719 0R0402-PAD-1-GP — HDMI_DATA1# R_C
A00 20160302

R5701 150R2J-L1-GP-U

HDMI_DATA1 R — R5718 0R0402-PAD-1-GP — HDMI_DATA1 R_C
A00 20160302

HDMI CONN

5V_HDMI_S5

C5703 SCD1U16V2KX-3GP

HDMI1

	18 +5V_POWER	SCL 15	DDC_CLK_HDMI
		SDA 16	DDC_DATA_HDMI
HDMI_DATA0 R_C	7 TMDS_DATA0+		
HDMI_DATA0# R_C	9 TMDS_DATA0-	CEC 13	
HDMI_DATA1 R_C	4 TMDS_DATA1+	DDC/CEC_GROUNG 17	
HDMI_DATA1# R_C	6 TMDS_DATA1-	HOT_PLUG_DETECT 19	
HDMI_DATA2 R_C	1 TMDS_DATA2+		
HDMI_DATA2# R_C	3 TMDS_DATA2-	RESERVED#14 14	
	8 TMDS_DATA0_SHIELD		
	5 TMDS_DATA1_SHIELD		
	2 TMDS_DATA2_SHIELD		
		GND 20	
	11 TMDS_CLOCK_SHIELD	GND 21	
HDMI_CLK R_C	10 TMDS_CLOCK+	GND 22	
HDMI_CLK# R_C	12 TMDS_CLOCK-	GND 23	

HDMI (A_Type)

SKT-HDMI23-147-GP
022.10025.00F1

HPD_HDMI_CON

69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend

5V_S5 — AFTP5701 — R5705 0R0603-PAD-1-GP-U — 5V_HDMI_R_S5 — F5701 POLYSW-1D1A6V-9-GP-U — 5V_HDMI_S5
A00 20160301

For DIODE in case of leakage from HDMI1

69.48001.081
2ND = 69.50011.081
3RD = 69.50013.101

3D3V_S0

84.T3904.H11

Q5702 LMBT3904LT1G-GP

B HDMI_HPD_B 2 — R5708 150KR2F-L-GP 1

R5707 200KR2F-L-GP DY

A00 20160302

[8] CPU_DP1_HPD — R5722 0R0402-PAD-1-GP — HDMI_HPD_E

[24] HDMI_EC_DET# — R5723 0R2J-2-GP DY

R5702 10KR2J-3-GP

3D3V_S5

R5711 10KR2J-3-GP

4th = 84.2N702.W31
3rd = 84.07002.I31
2ND = 84.2N702.031
84.2N702.J31
2N7002K-2-GP

[24] HDMI_EC_DET# — R5713 0R0402-PAD-1-GP — HDMI_EC_DET# C
A00 20160302

Q5704

HPD_HDMI_CON_C — R5712 0R0402-PAD-1-GP — HPD_HDMI_CON
A00 20160302

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Drax SKL Y | Rev: A00

Date: Tuesday, March 22, 2016 | Sheet 57 of 109

SSID = Display Port

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved) Display Port*	
Size	Document Number: *Drax SKL Y*	Rev: *A00*
Date: Thursday, March 17, 2016	Sheet 58 of 109	

SSID = DVI

Blanking

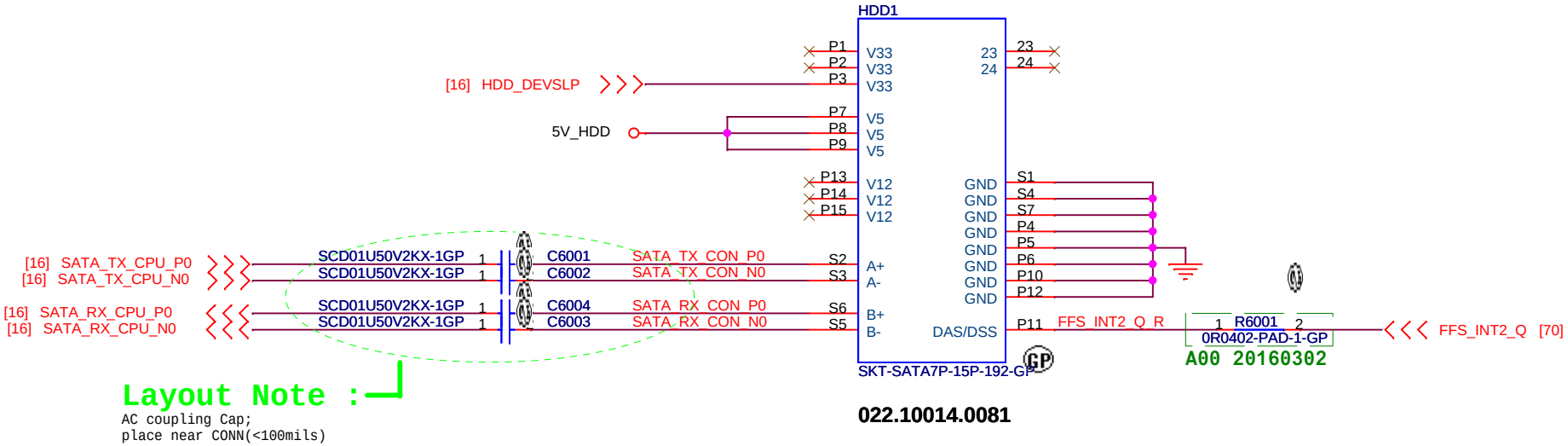
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved) DVI*	
Size	Document Number: *Drax SKL Y*	Rev: *A00*
Date: Thursday, March 17, 2016	Sheet 59 of 109	

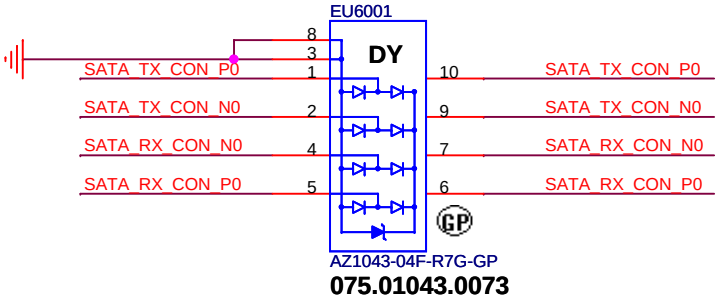
SSID = SATA

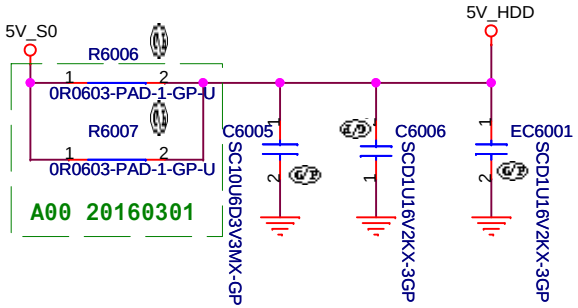
SATA HDD Connector



Layout Note :

AC coupling Cap;
place near CONN(<100mils)

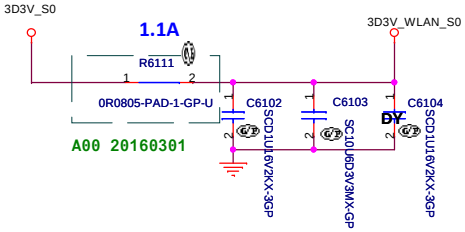


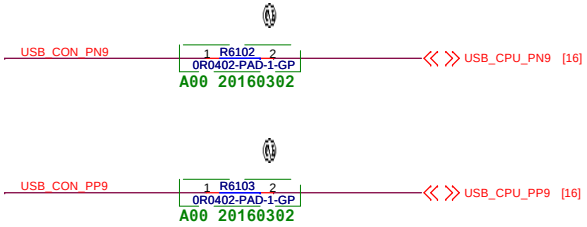


<Core Design>

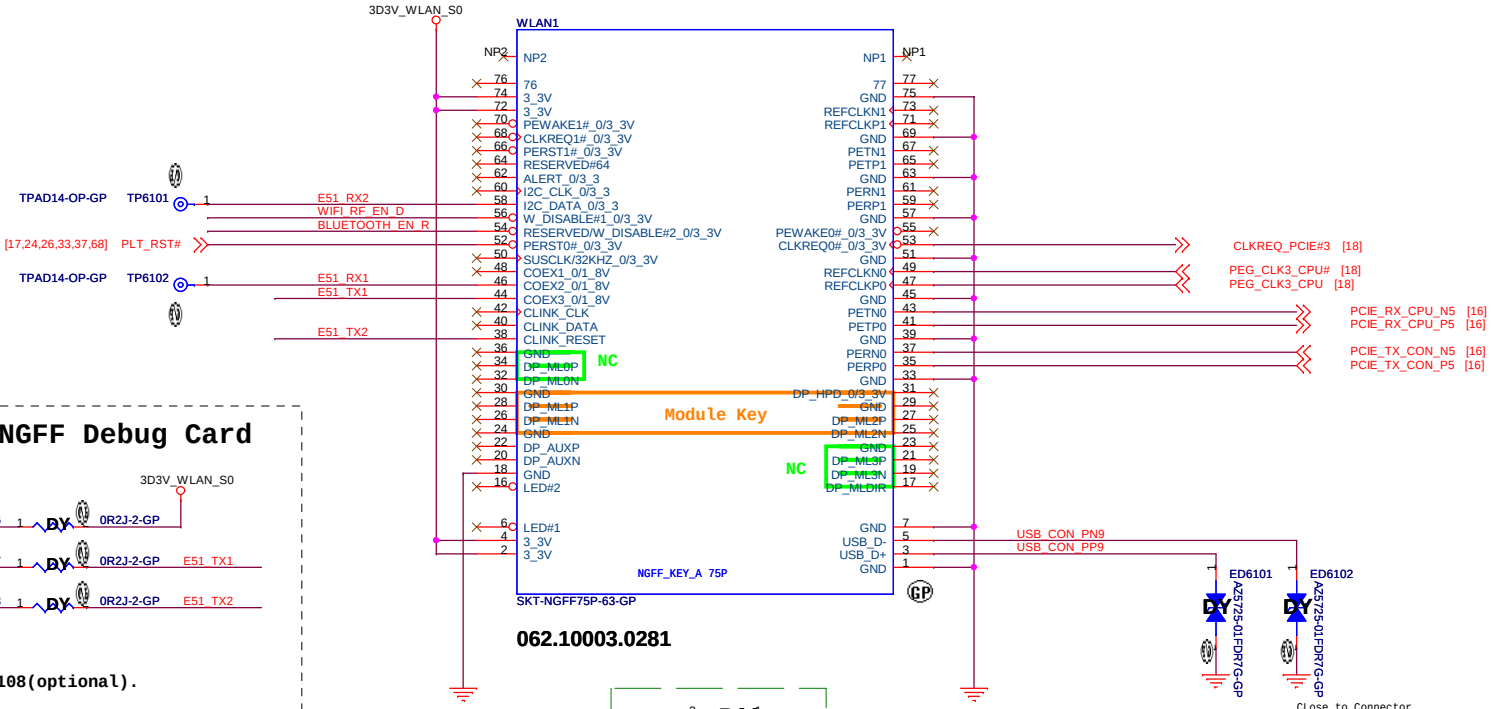
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: Drax SKL Y	Rev: A00
Date: Tuesday, March 22, 2016	Sheet 60 of 109	

SSID = WLAN

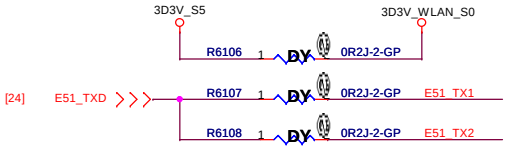




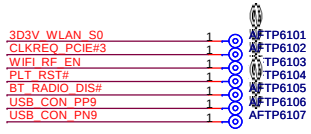
Mini Card Connector(802.11a/b/g)

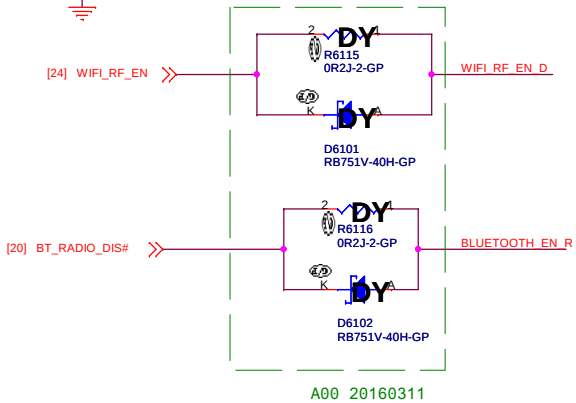


Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	WLAN	
Size	Document Number: Drax SKL Y	Rev: A00
Date: Tuesday, March 22, 2016	Sheet 61 of 109	

SSID = WWAN

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved) WWAN***	
Size	Document Number: ***Drax SKL Y***	Rev: ***A00***
Date: Thursday, March 17, 2016	Sheet 62 of 109	

SSID = SSD-NGFF

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	eMMC	
Size A4	Document Number Drax SKL Y	Rev A00
Date: Thursday, March 17, 2016	Sheet 63 of 109	

SSID = LED / PWRBTN

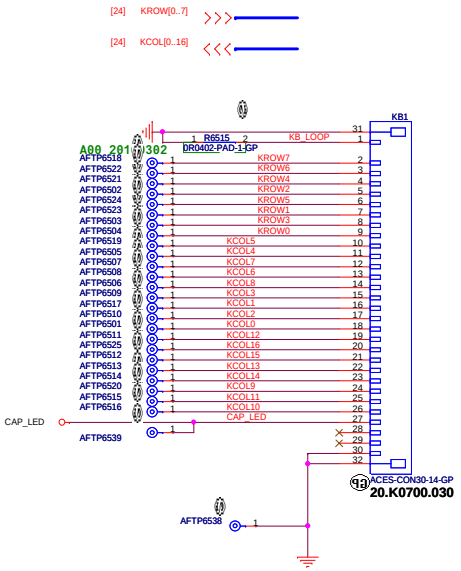
Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***LED / PWRBTN***	
Size: A4	Document Number: ***Drax SKL Y***	Rev: ***A00***
Date: Thursday, March 17, 2016	Sheet 64 of 109	

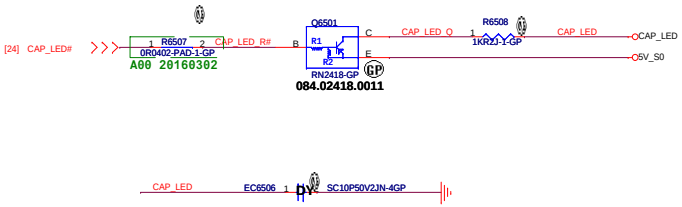
Main Func = KB



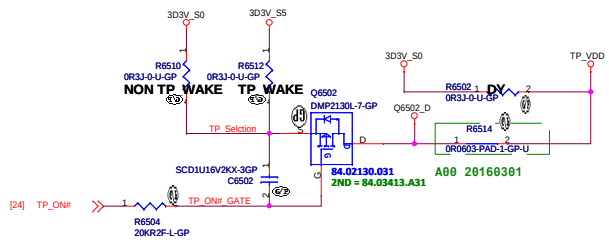
PIN#	SIGNAL
1	Diag_Loop=GPIO_1(TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

CAP LED Control

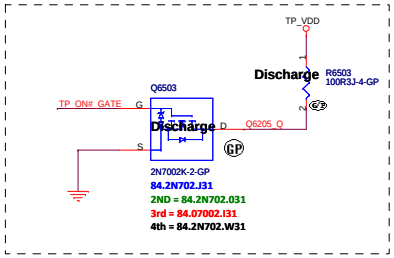
LOW actived from KBC GPIO



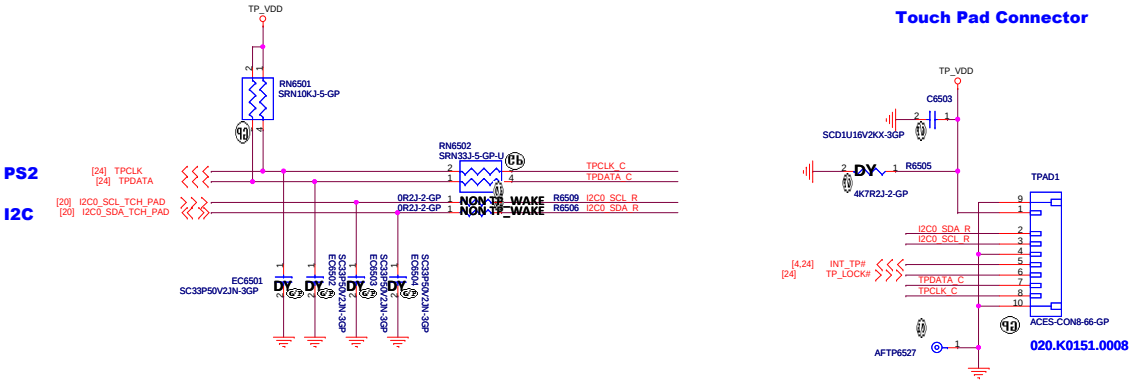
Main Func = TPAD

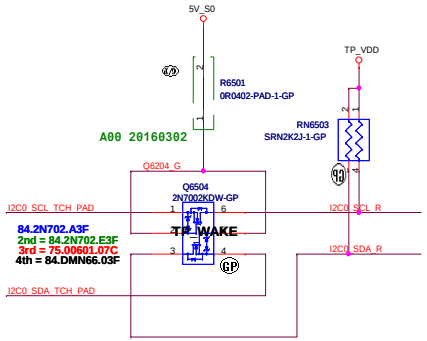


TP_VDD Discharge Circuit

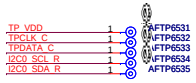


Touch Pad Connector

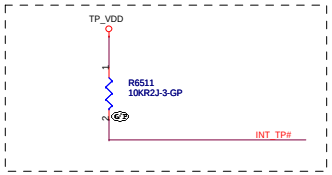




Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad
Size: C
Document Number: Drax SKL Y
Rev: A00
Date: Tuesday, March 22, 2016
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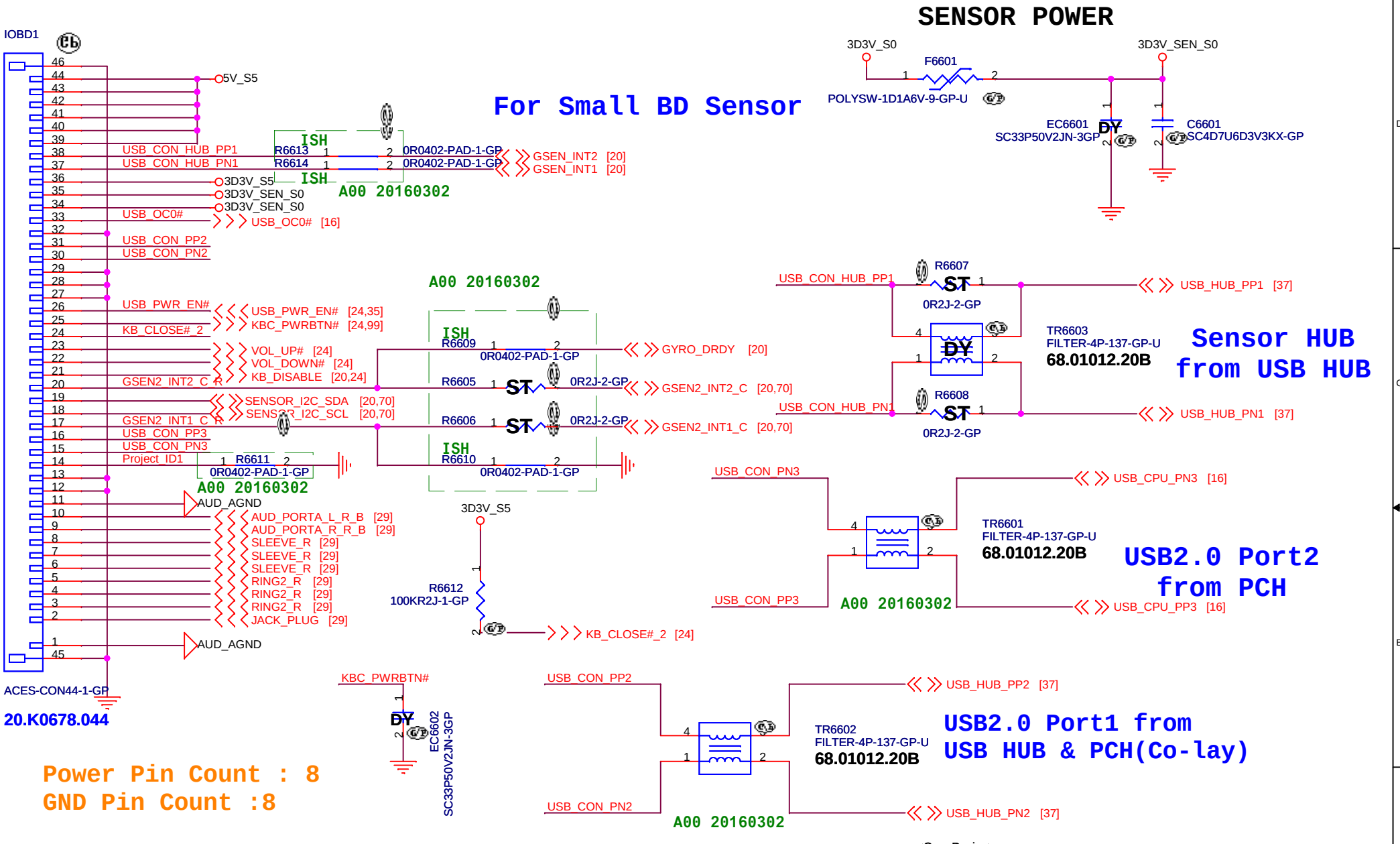

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board CONN*

Size	Document Number	Rev
A4	Drax SKL Y	A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

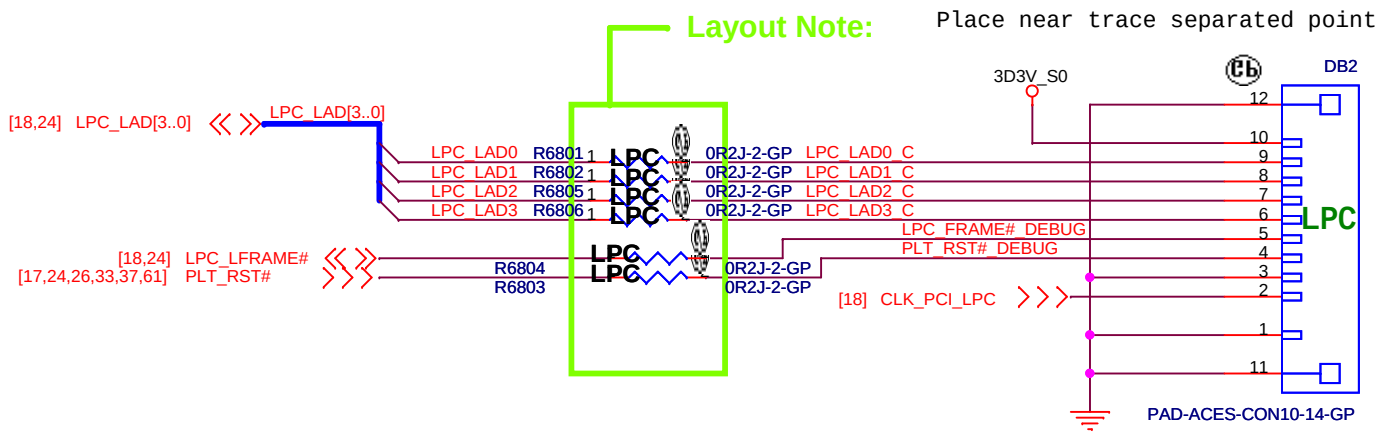
Hall Sensor

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

Date: Thursday, March 17, 2016 Sheet 67 of 109

SSID = Debug CONN

LPC Debug Port



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

A00 20160302

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Debug CONN		
Size A4	Document Number *Drax SKL Y*	Rev *A00*
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SSID = Sensor

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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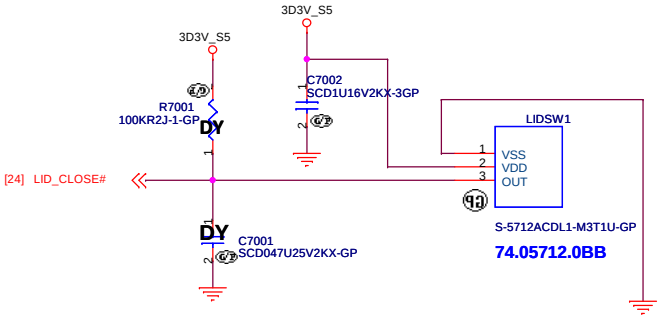
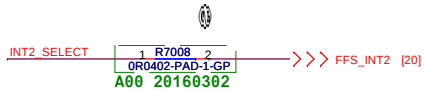
Title	Sensor	
Size A4	Document Number Drax SKL Y	Rev A00
Date: Thursday, March 17, 2016	Sheet 69 of 109	

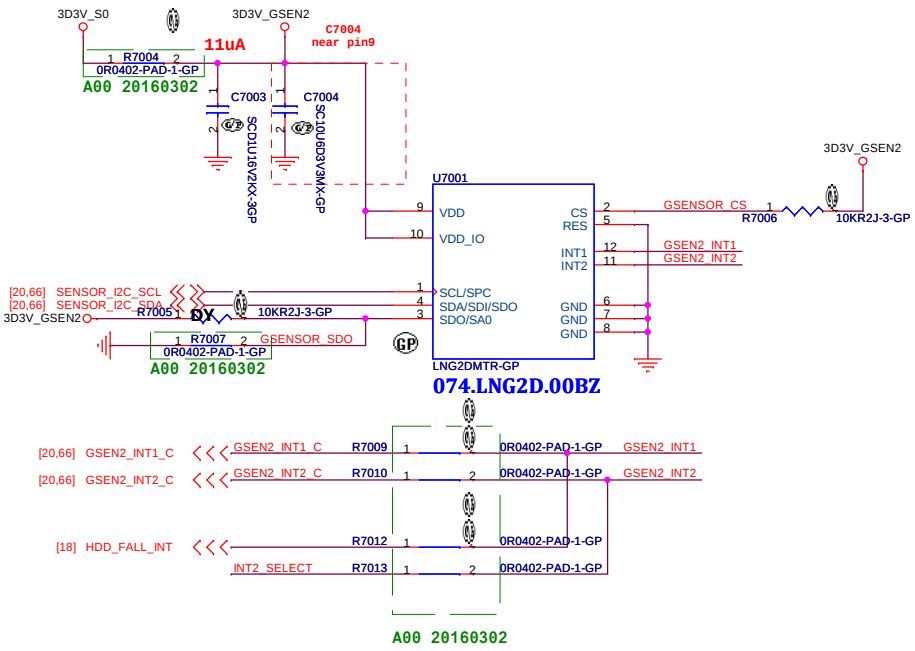
Main Func = Hall Sensor

LID sensor

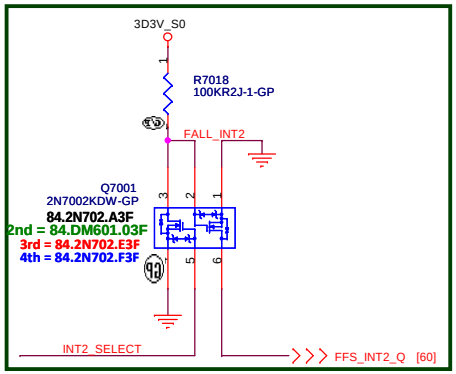




Free Fall Sensor + G Sensor



Please help to close with U6602



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Thunderbolt (1/5)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

Date: Thursday, March 17, 2016 | Sheet 71 of 109

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)Thunderbolt (2/5)***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
Date: Thursday, March 17, 2016	Sheet 72 of 109	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Thunderbolt (3/5)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

Date: Thursday, March 17, 2016 | Sheet 73 of 109

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Thunderbolt (4/5)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

Date: Thursday, March 17, 2016 | Sheet 74 of 109

Blanking

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***(Reserved)Thunderbolt (5/5)***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
Date: Thursday, March 17, 2016	Sheet 75 of 109	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)GPU (1/5) PEG***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)GPU (2/5) DIGITAL***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)GPU (3/5) VRAM***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)GPU (4/5) GPIO***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)GPU (5/5) PWR/GND***	
Size A4	Document Number ***Drax SKL Y***	Rev ***A00***
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)VRAM1,2 (1/4)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)VRAM3,4 (2/4)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)VRAM5,6 (3/4)

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)VRAM7,8 (4/4)***

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Blanking

<Core Design>

Wistron Corporation
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Title
(Reserved)VGA_CORE

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Title: ***(Reserved)DISCRETE VGAPOWER***

Size	Document Number	Rev
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Title

(Reserved)

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Title: ***(Reserved)***

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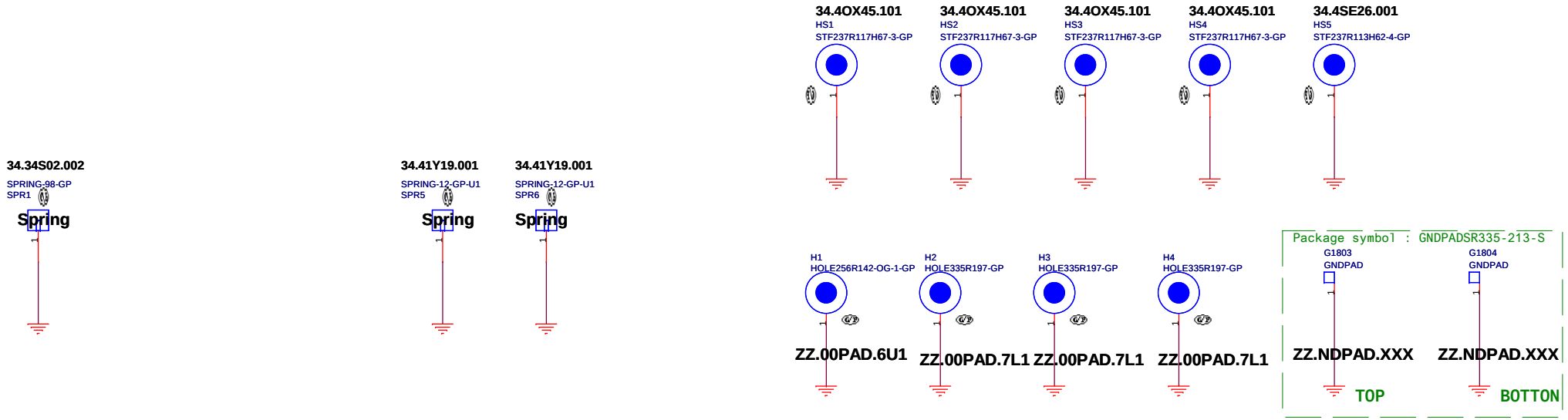
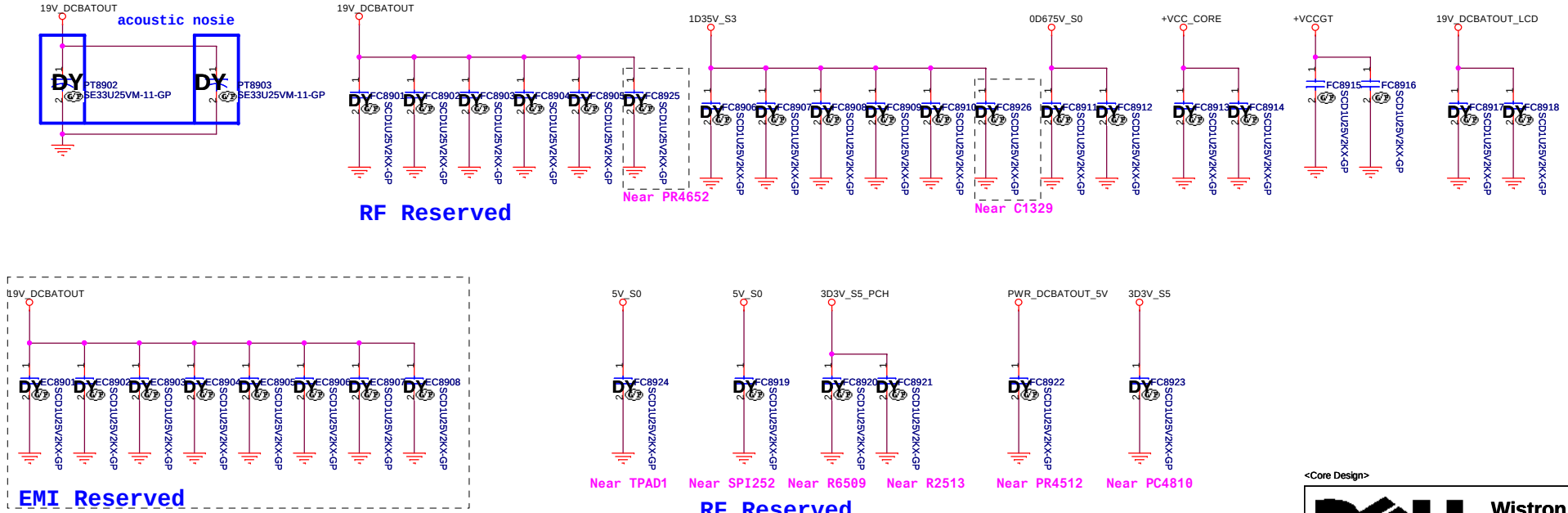
Main Func = UnusedParts



Main Func = EMICapacitors



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Title: ***UNUSED PARTS/EMI Capacitors***

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Title: ***(Reserved)NFC Connector***

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Title	(Reserved) TPM	
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Title
(Reserved)Finger Print

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Title
(Reserved)Express Card

Size	Document Number	Rev
A4	***Drax SKL Y***	***A00***

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Title	***(Reserved)Smart Card Socket***	
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Title: ***(Reserved)SW GFX eDP***

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SSID = DEBUG PORT

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Title	CPU_XDP	
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Title	***(Reserved)LAN***	
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Title: ***(Reserved)LAN SWITCH***

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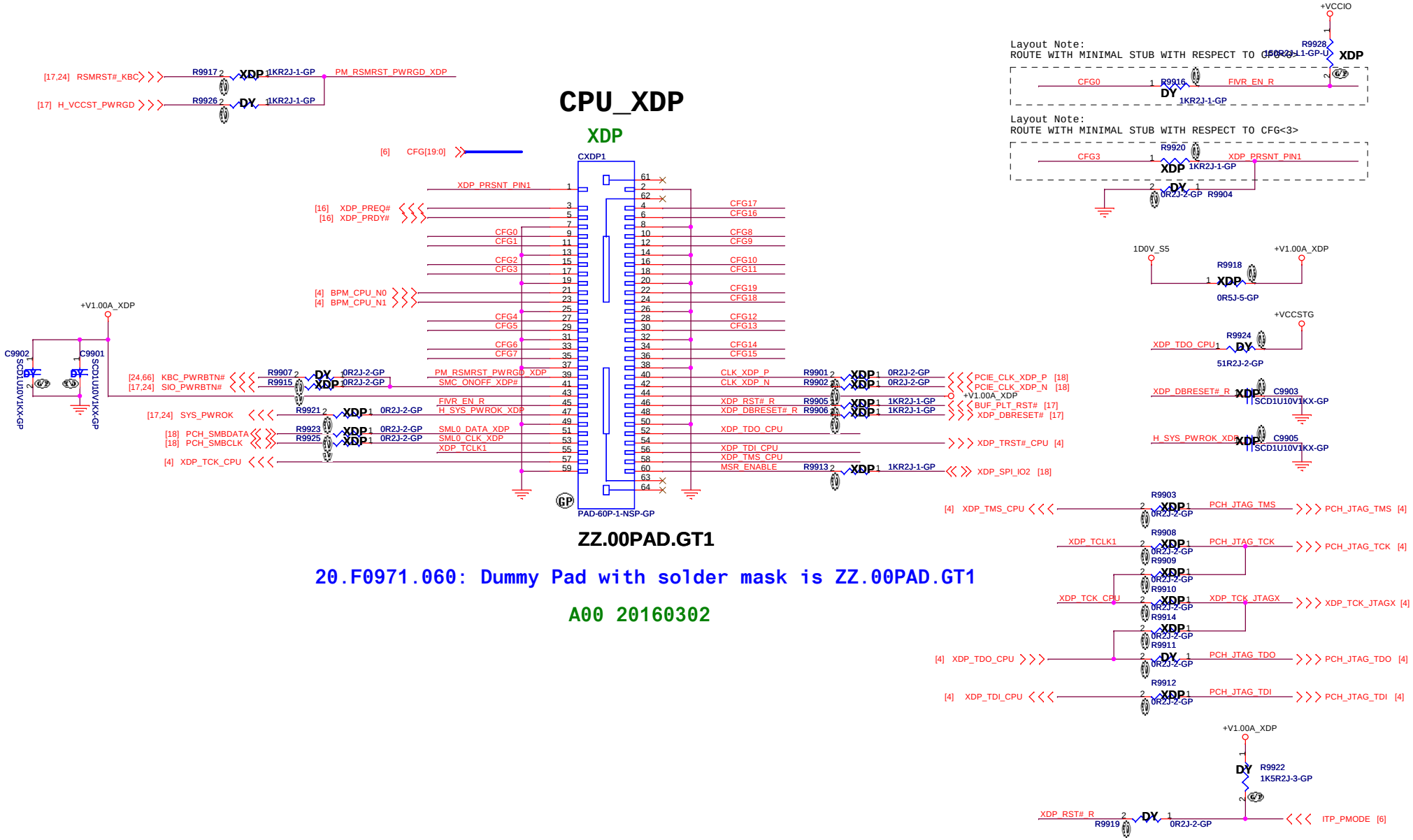
SSID = XDP CONN

CPU_XDP

XDP



ZZ.00PAD.GT1

20.F0971.060: Dummy Pad with solder mask is ZZ.00PAD.GT1

A00 20160302

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Title: CPU XDP		
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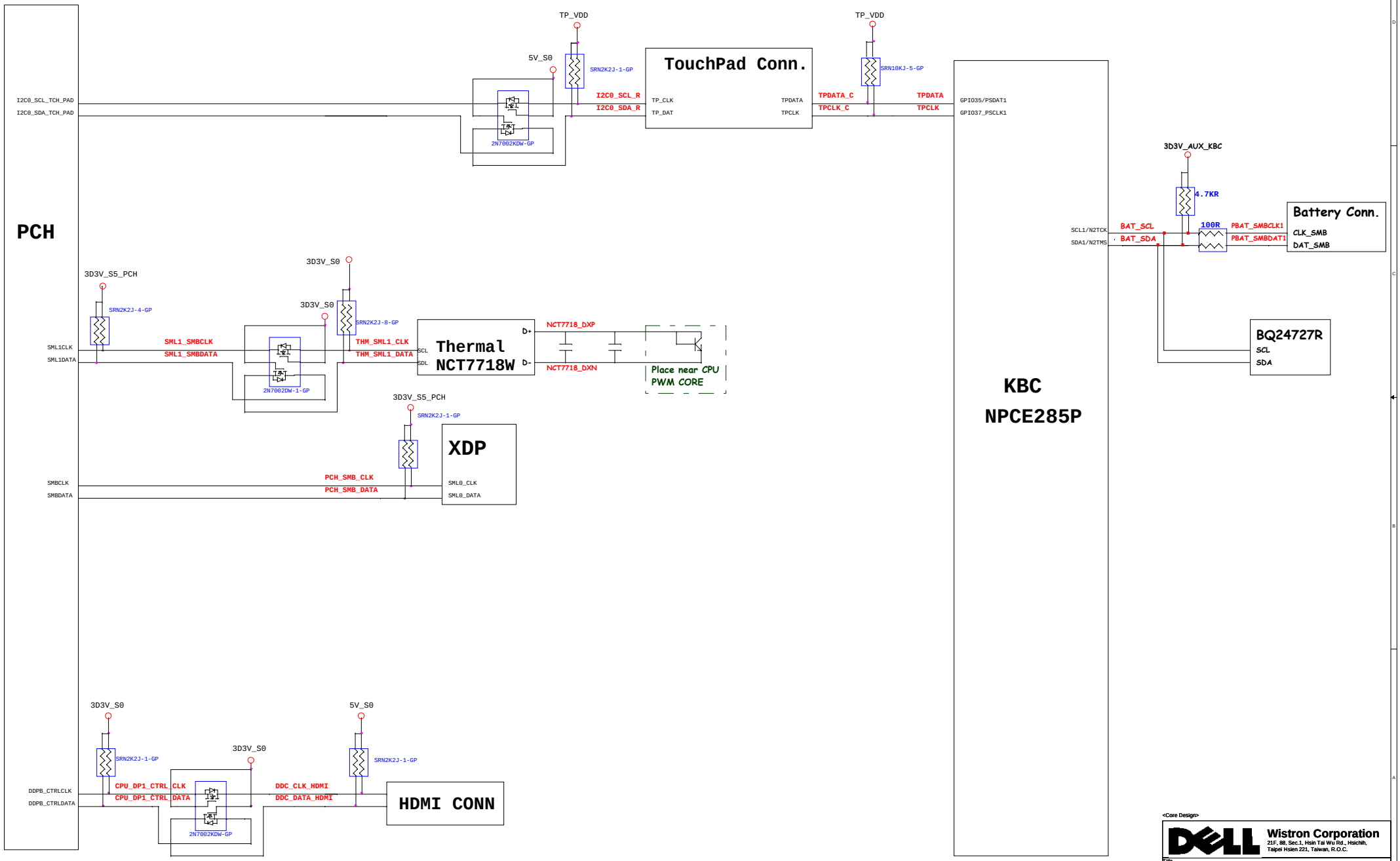
SMBus Block Diagram



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Title: SMBUS Block Diagram

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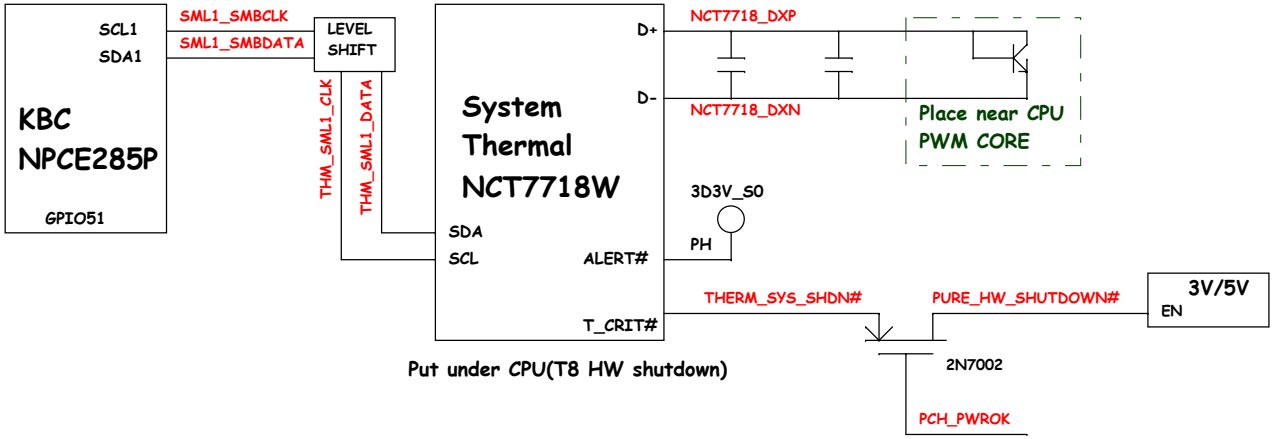
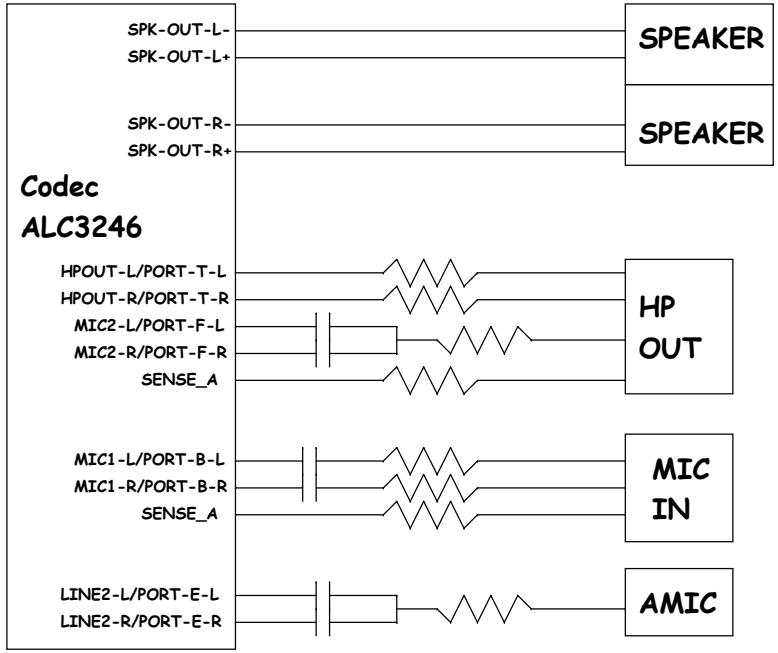
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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Title: *Change History-01*

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Title: *Change History-02*

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Title: ***Change History-02***

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